cadence™

Allegro®
Design Entry HDL Tutorial

Series L and XL

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Contents

1

Introduction to Design Entry HDL Tutorial

This chapter contains the following information:

Overview

This tutorial demonstrates the major tasks involved in creating a schematic. Design Entry HDL is the tool used for Design Entry (also known as Design Capture) in the Printed Circuit Board design flow. With Design Entry HD, you can create a project, place components (parts), connect parts, name signals, add ports, and save designs.

When you save a design, Design Entry HDL checks for errors and helps you locate the spots on the schematic where connectivity errors have occurred.

There are two menu use models, post-select and pre-select, in which you can work in Design Entry HDL. In post-select use model, you first select the command and then the schematic component is selected. In the pre-select use model, first the schematic component is selected and then the command is selected.

For example, you want to delete a schematic component. The steps in the post-select use model are:

- Choose *Edit – Delete*
- Select the component to be deleted

In the pre-select use model the steps are:

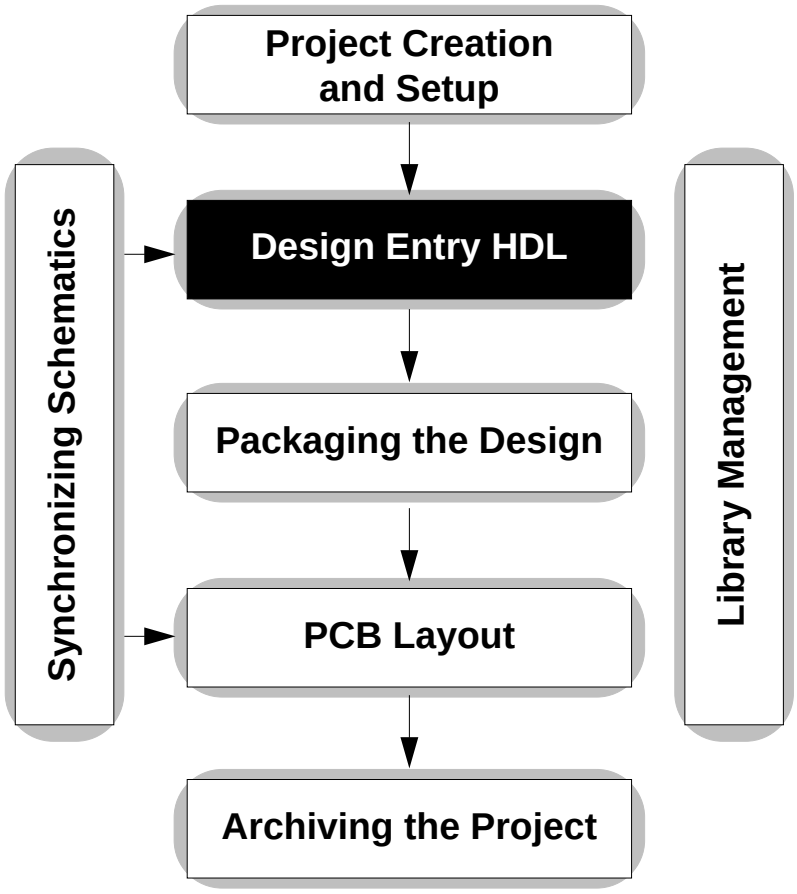
- Choose the component to delete
- Choose *Edit – Delete*

By default Design Entry HDL supports the post-select model for schematic operations. This tutorial is in the post-select mode. To know about the pre-select mode, see Setting the Pre-Select Use Model on page 33.

Design Entry HDL in the PCB Flow

This tutorial explains how to create a schematic design by using Design Entry HDL.

Design Entry HDL helps you capture the design of a Printed Circuit Board (PCB) in the schematic form. This design is packaged and opened in Allegro PCB Editor to perform the placement and routing. The completed board design is then sent to manufacturing for the production of PCB. The following figure illustrates the overall design flow for printed circuit boards and highlights the space where Design Entry HDL fits in.



How To Use this Tutorial

This tutorial provides hands-on exercise in creating a design using Design Entry HDL. To understand how you can use Design Entry HDL to create designs, you should follow the steps in the sequence they appear in the chapters of this tutorial.

Important

The Design Entry tutorial is written in the flow in which a schematic is usually created. Follow the steps in the tutorial in the order in which they are covered. This way you easily assimilate the methods for creating a schematic. You should complete the tutorial in one session, which will require approximately 8 hours of effort. If you plan to complete the tutorial across days, then complete at least one chapter in each session.

Before using the tutorial, you need to unzip the file <*your_inst_dir*>/doc/concepthdl_tut/tutorial_examples/local_lib.zip on Windows NT, or <*your_inst_dir*>/doc/concepthdl_tut/tutorial_examples/local_lib.tar.z on UNIX, and save it locally. The local_lib library, which is a directory, contains the parts that you will use while creating a schematic using this tutorial.

Brief Outline of Chapters

The Design Entry HDL Tutorial is divided into three chapters:

- Creating a Project on page 9

  This chapter explains what a project is. It also explains libraries, the `cds.lib` file, and the project file. This chapter contains procedures to create and set up a project.

- Creating a Schematic: Basics on page 29

  This chapter explains the basic tasks involved in creating a simple multi-page schematic. The tasks covered include adding parts, connecting parts, saving and checking the design, creating buses, tapping buses, and adding physical information.

- Creating a Schematic: Advanced on page 81

  This chapter explains the advanced tasks you perform while creating hierarchical designs. It explains the two methods that may be followed for creating a hierarchical design. This is followed by procedures to create a hierarchical design using the top-down and the bottom-up methods. The chapter also explains the method to package the design. If errors are detected while packaging, *Global Find* is used to locate the components. To edit the properties attached to components, the Attributes dialog box is used. After you have fixed the errors, re-packaging needs to be done.

2

Creating a Project

This chapter contains the following information:

Overview

The first task you perform in designing a PCB is to create a project. A design project is the encapsulation of paths to libraries, part tables, tool settings, global settings, view directory names, and other related settings for designing a PCB to required specifications.

A design project consists of the following:

- Reference libraries
- Local libraries (design libraries)
- `cds.lib` file
- Project file (`.cpm` file)

The following sections provide more details about these components.

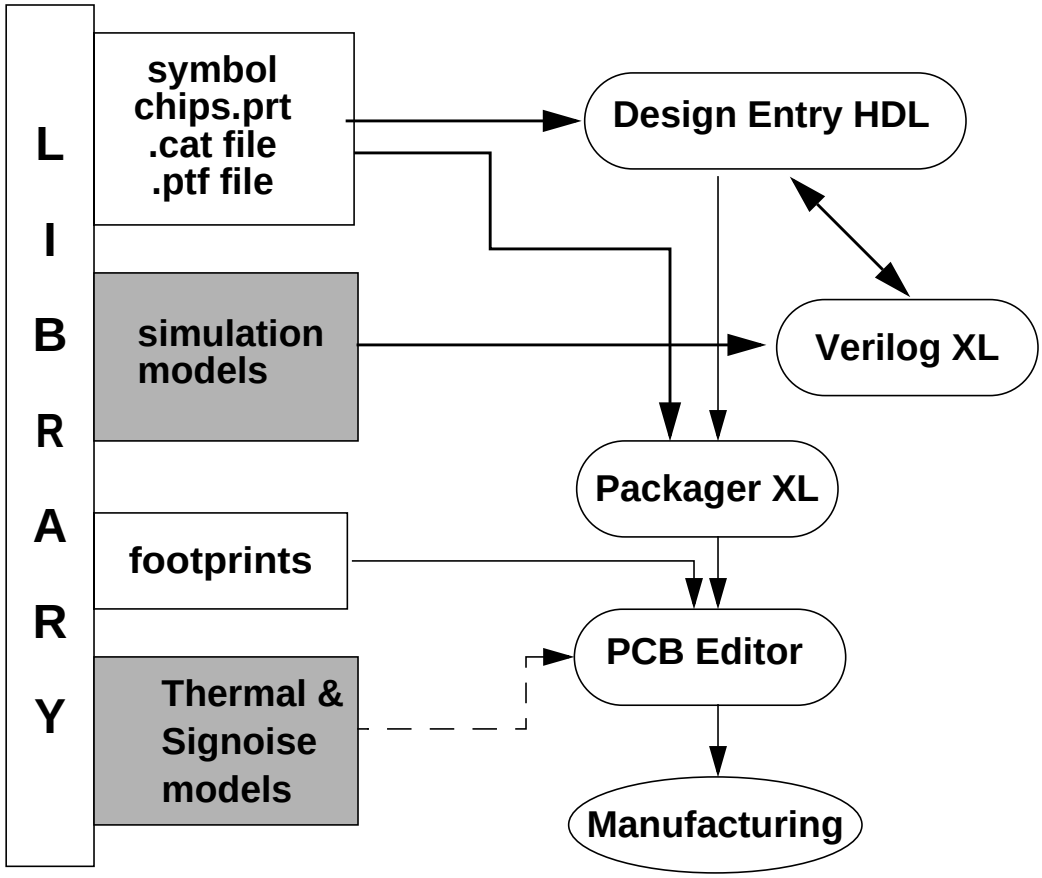
What are Libraries?

You begin the design process by creating a logic design (schematic) and then a board-level design that translates the logic design into a manufacturable entity. To accomplish this process, tools need a *software* representation of the various parts to be used in the design. The representations of these parts are organized into libraries.

The different tools used in the various stages of the design flow, need different views or information about the same part. Some of these views are schematic, footprint, and simulation.

These views are organized into several libraries. For example, footprints of various parts are consolidated into a single layout library.

The library organization for Cadence Board Design tools is as follows:



- Schematic libraries

  These libraries contain views for design entry, or schematic creation. The information contained in these views includes logical symbols (graphical representations of the part), pinouts, and packaging information.

- Layout libraries

  These libraries contain the footprints that correspond to the physical parts specified in schematic libraries. These libraries are required at the layout stage of the design flow.

- Simulation Libraries

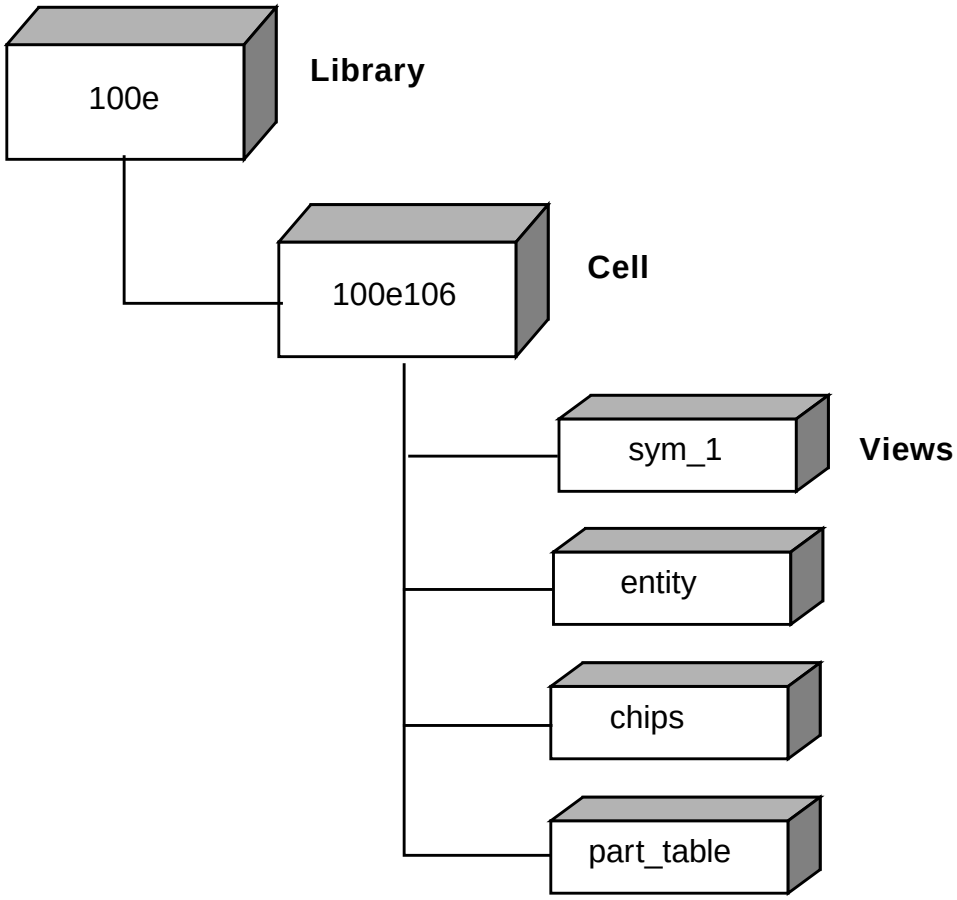
  These libraries model the behavior of the part in the Verilog or VHDL Hardware Description Languages. These libraries are required during the verification phase.

Cadence supplies a set of **reference libraries** that contain views of parts belonging to several logic families. The `Standard Library` is an example of a reference library. These libraries are usually stored in an area to which you do not have Write permissions and are managed by a librarian.

The Cadence Standard Library is located at <*`your_inst_dir`*>`/share/library`.

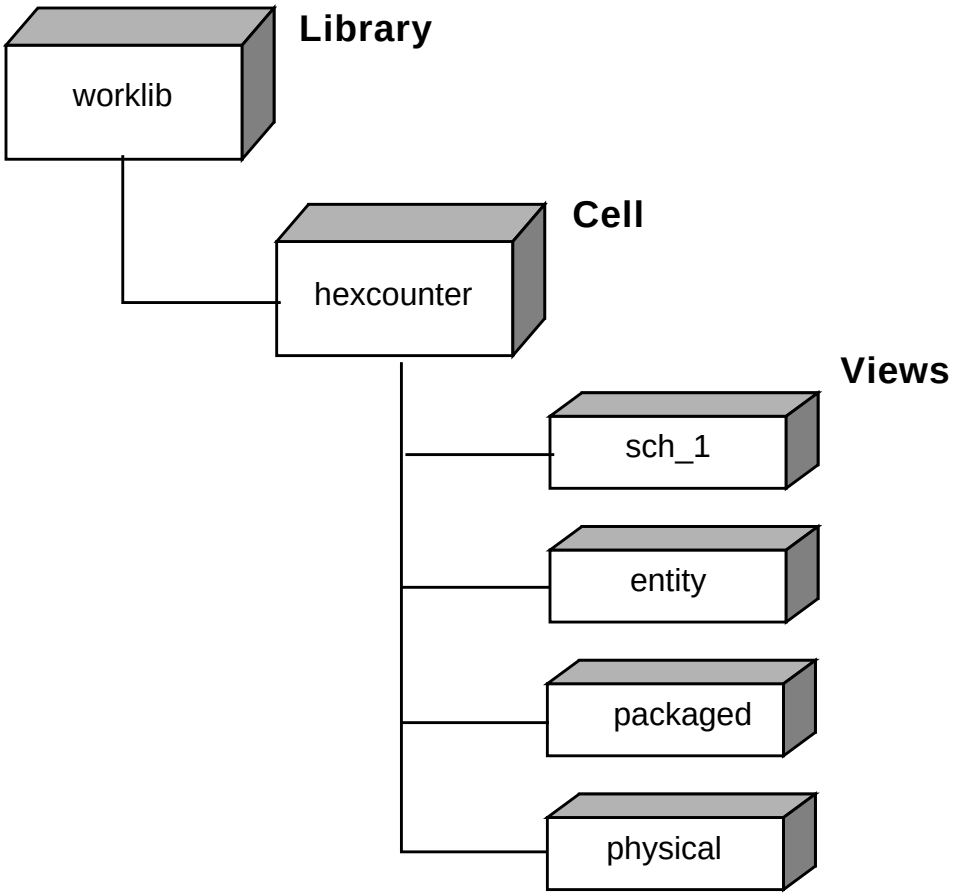
The following table describes each view within a part in a reference library.

View Name	Description
sym_1	Contains the schematic symbol
entity	Contains a master pin list. This view is generated when you save a schematic symbol.
chips	Maps the logical part to the physical package.
part_table	Contains additional properties which helps customize the part for a company



Note: All the libraries that are referred to in this tutorial would be available to you only if you install the Cadence Libraries CD.

Local libraries (also known as design libraries) are used by designers at the local project level. You can import reference libraries and change them to suit your design requirements or you can use reference libraries as they are.



The following table describes each view in a design library.

View	Description
sch_1	Contains the schematics
entity	Contains a high-level description of the design
packaged	Contains the results of packaging
physical	Contains component footprints

What is a cds.lib File?

Design Entry HDL is a by-reference schematic editor. This means that Design Entry HDL references all parts in the schematic from various libraries that reside at the reference or local area.

The *cds.lib* file defines all the libraries used in your schematic design and maps them to their physical locations.

Contents of a typical *cds.lib* file:

```
DEFINE 54alsttl ../../library/54alsttl
DEFINE 54fact ../../library/54fact
DEFINE tutorial_lib worklib
INCLUDE $CONCEPT_INST_DIR/share/cdssetup/cds.lib
DEFINE local_lib local_lib
```

What is a Project File

When you create a new project, Allegro Project Manager creates a project file called `<projectname>.cpm` in the project directory. The `<projectname>.cpm` file includes the following setup information for your project:

- The name of the top-level design and the library in which it is located
- The list of project libraries
- The name and location of the text editor for editing text files from Cadence tools
- The location of the temporary directory where tools generate intermediate data
- Setup directives for individual tools, such as Design Entry HDL, Packager-XL, Programmable IC, and PCB Editor
- Directives for customizing the Project Manager (a customized Tools menu or customized flows)
- The current session name

Creating a Project

To create a project, you use Project Manager.

1. Start Project Manager.
   - ❑ On Windows NT, choose *Start – Programs – Allegro SPB 15.7 – Project Manager*.
   - ❑ On UNIX, type `projmgr &` in a shell window.
2. Select the appropriate license.

   Project Manager appears.

Click to create a new design

The *Open Project* button is used to open an existing project. To create a new project, click the *Create Design Project* button.

In this chapter, you will create a new project called `tutorial`. The project files will be stored in the `Designs` folder on the `D:\` drive.

1. To start creating the project, click *Create Design Project*.

   The New Project Wizard appears.

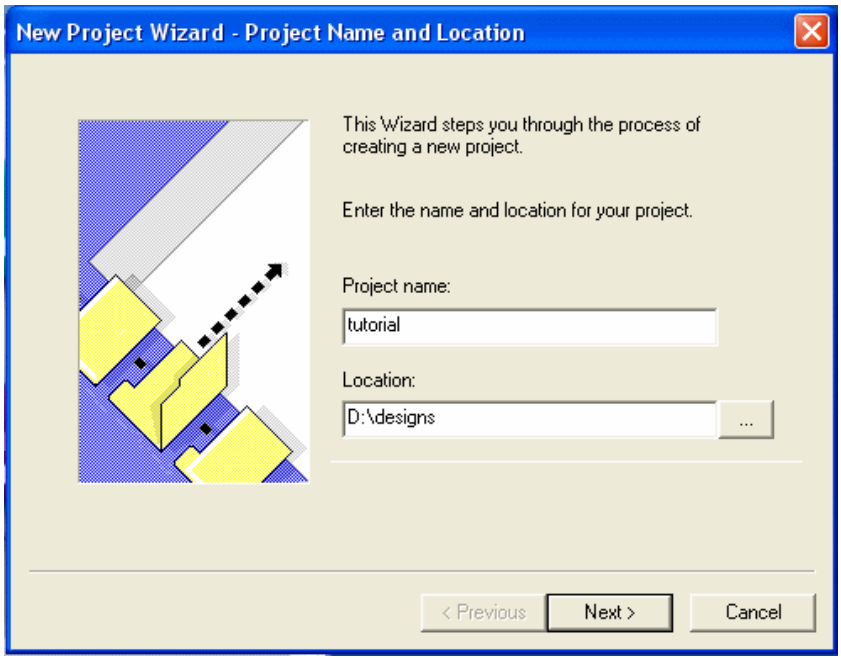
   In the first step of the wizard, specify the project name and the location where the project files should be created.

2. Enter the project name as `tutorial`.

   The wizard will create a project file called `tutorial.cpm`.

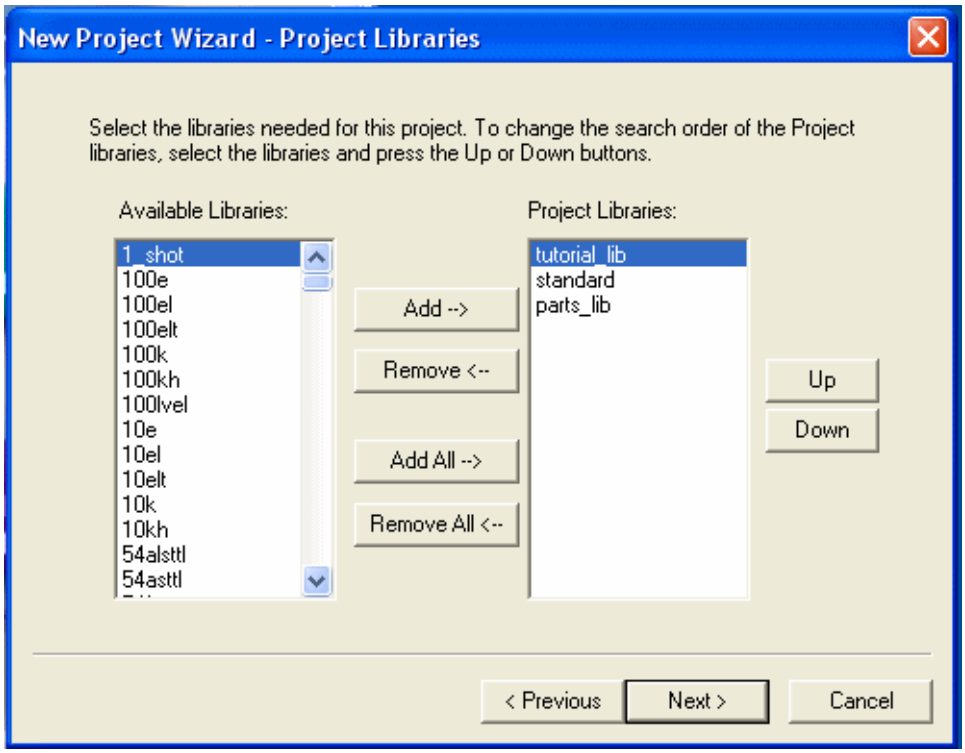
3. Enter the location as `D:\Designs`.

   If the directory Designs does not exist, Project Manager creates it. You can also use the browse button to specify the location of the project.



4. Click *Next*.

The New Project Wizard - Project Libraries page appears.



The *Project Libraries* page allows you to select the libraries for your project from the list of available libraries. By default, a library named `tutorial_lib` (`<project_name>_lib`) is added to the Project Libraries list. This is the logical library name. After project is created, the physical name of this library will be `worklib`. The `cds.lib` file defines `tutorial_lib` as `worklib`.

The `Standard Library` is also added by default in the *Project Libraries* list.

Note: All the libraries listed in the above screen shot would be available to you only if you install the Cadence Libraries CD. To add other libraries to the Available Libraries list, you can edit the `cds.lib` file. For more information, see Adding Libraries Using Project Setup on page 22.

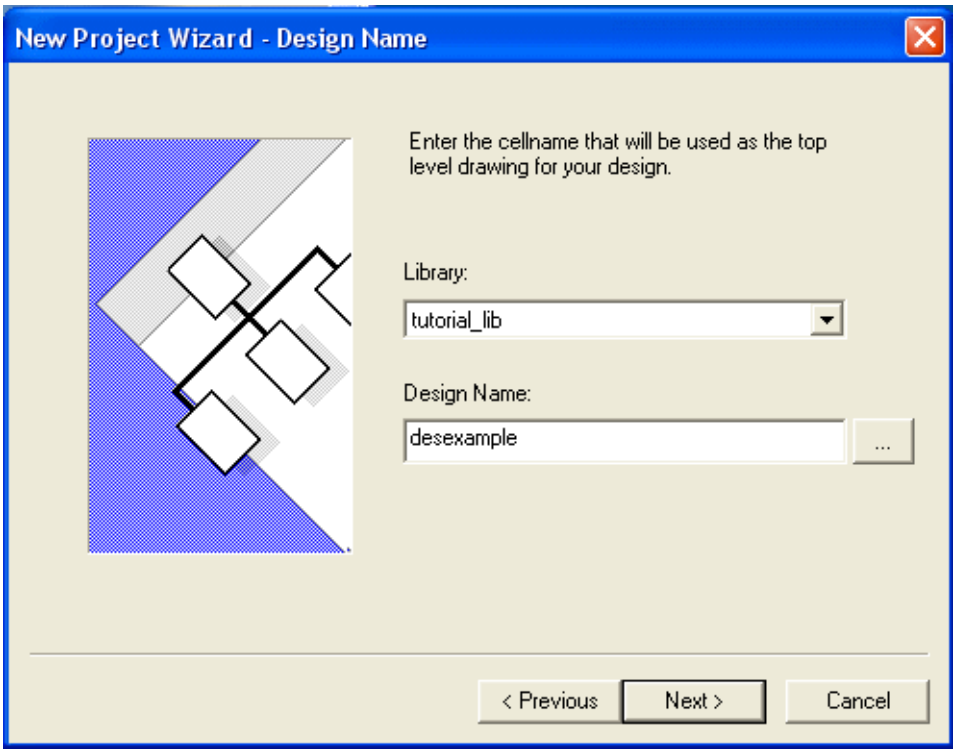
5. Click *Next*.

   The Design Name page appears.

6. Select *tutorial_lib* as the design library.

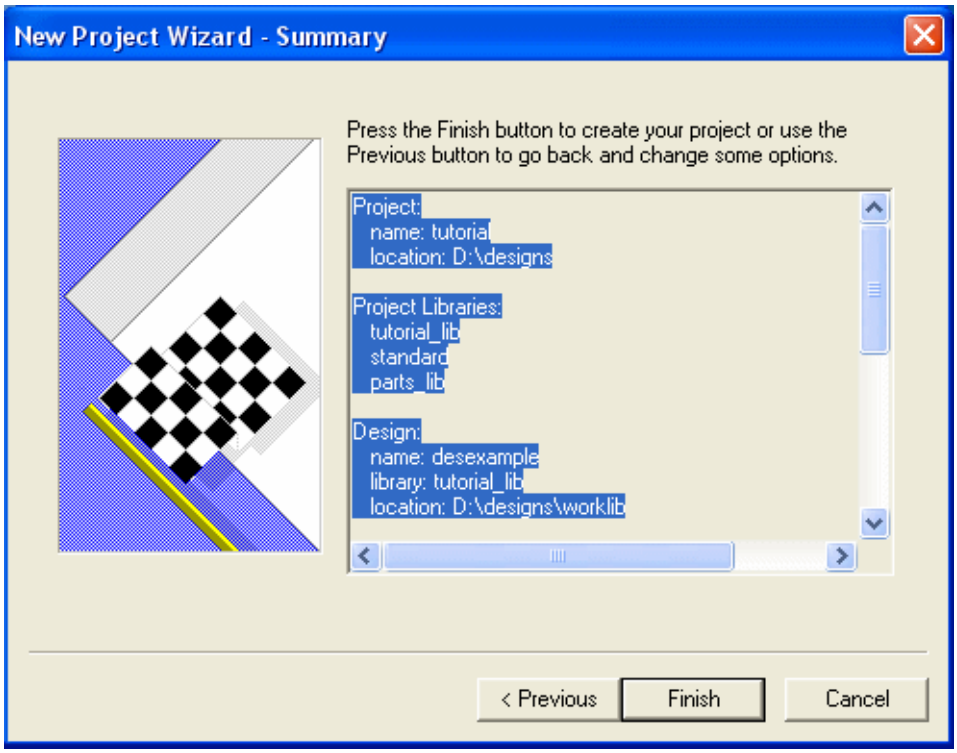
   The top-level design will be placed under the `tutorial_lib` library.

7. Type `desexample` as the top-level design name.



8. Click *Next*.

The Summary page appears.



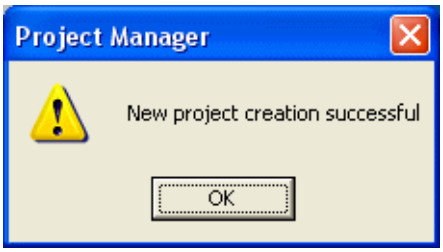
To modify the details, click *Previous* to go back to the previous steps.

9. Click *Finish*.

The following message is displayed.

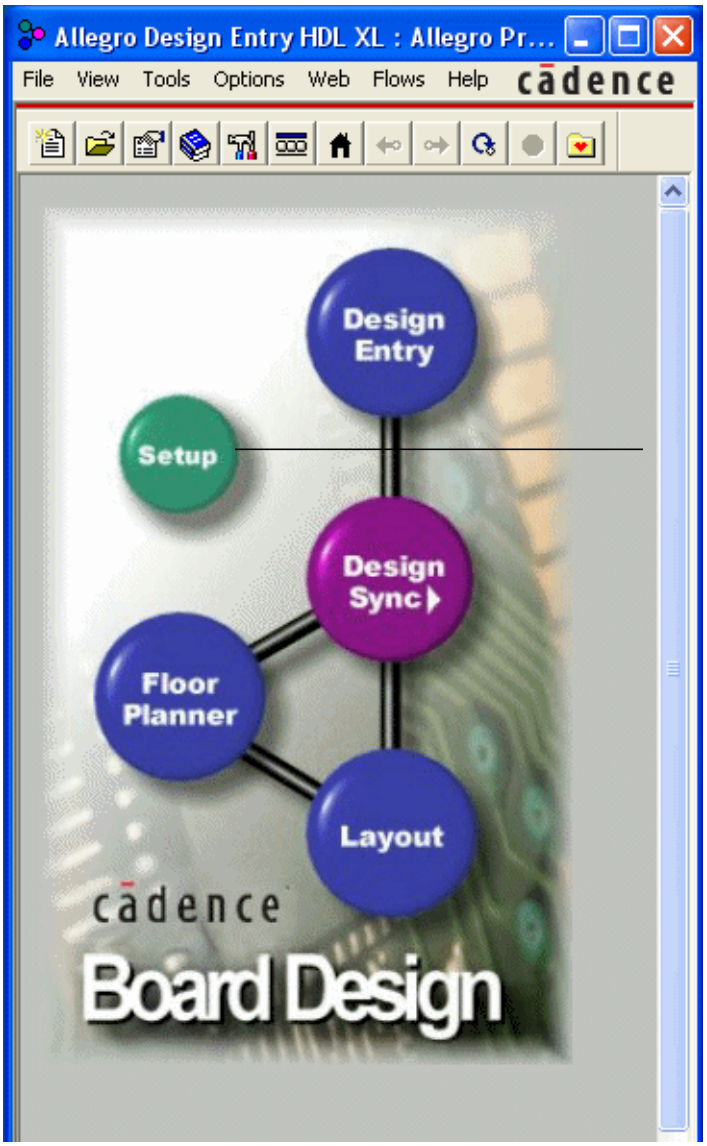
10. Click *Yes*.

Progress messages display and finally, a message confirms the new project creation.



11. Click *OK*.

Project Manager creates the project and displays the board design flow.



Click to complete setup tasks

Video

See the multimedia demonstration titled, *Creating a Project* for an example of the design project creation. The demonstration is available on SourceLink. The instructions to access this and other demonstrations on SourceLink are available on the *Legacy Demos* page of the Allegro Design Entry HDL Help System page. To launch the Help System page, choose *Help – Documentation* in Design Entry HDL, and click the *Demos* tab.

Adding Libraries Using Project Setup

After you have created a project using the New Project Wizard, you can make changes, such as adding new libraries and cells, to the project. In this section, you add the `local_lib` library to the list of Project Libraries.

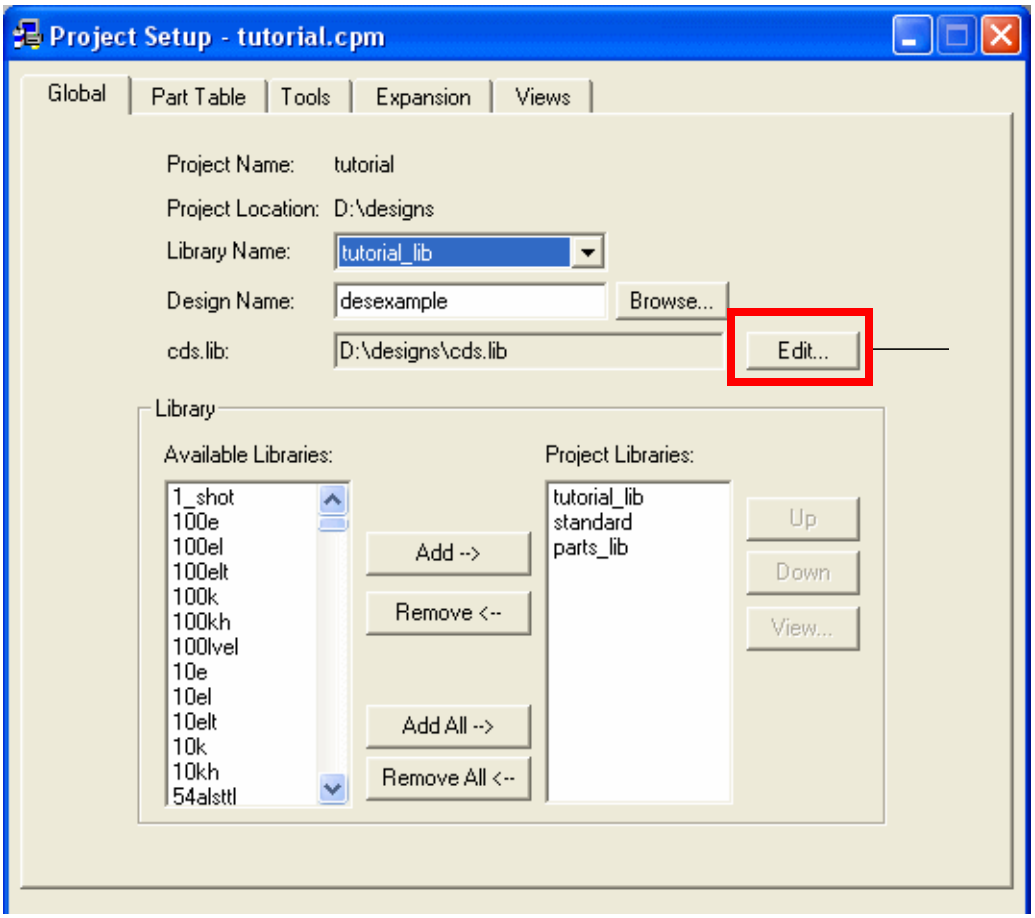
1. On Windows NT, unzip `local_lib.zip` available at `<your_inst_dir>/doc/concepthdl_tut/tutorial_examples` and extract the contents to `D:\Designs\local_lib`.

   On UNIX, uncompress and untar `local_lib.t.Z` available at `<your_inst_dir>/doc/concepthdl_tut/tutorial_examples` and extract the contents to `home/Designs/local_lib/`.

Note: The `local_lib` library is created only for the current tutorial and is not a standard library file.

2. Click the *Setup* icon in the Project Manager window.

The Project Setup dialog box appears.



Click here to edit the cds.lib file.

3. Click *Edit* next to the `cds.lib` field.

   Project Manager opens the `cds.lib` file in a text editor.

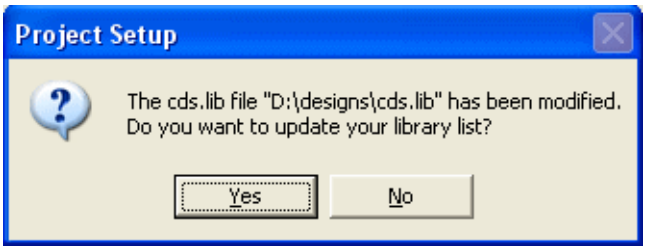
4. Enter the following line in the `cds.lib` file.

   ```
   DEFINE local_lib local_lib
   ```

   This line in the `cds.lib` file adds the `local_lib` library to the available libraries list.

5. Save and close the `cds.lib` file.

Project Manager displays the following message.

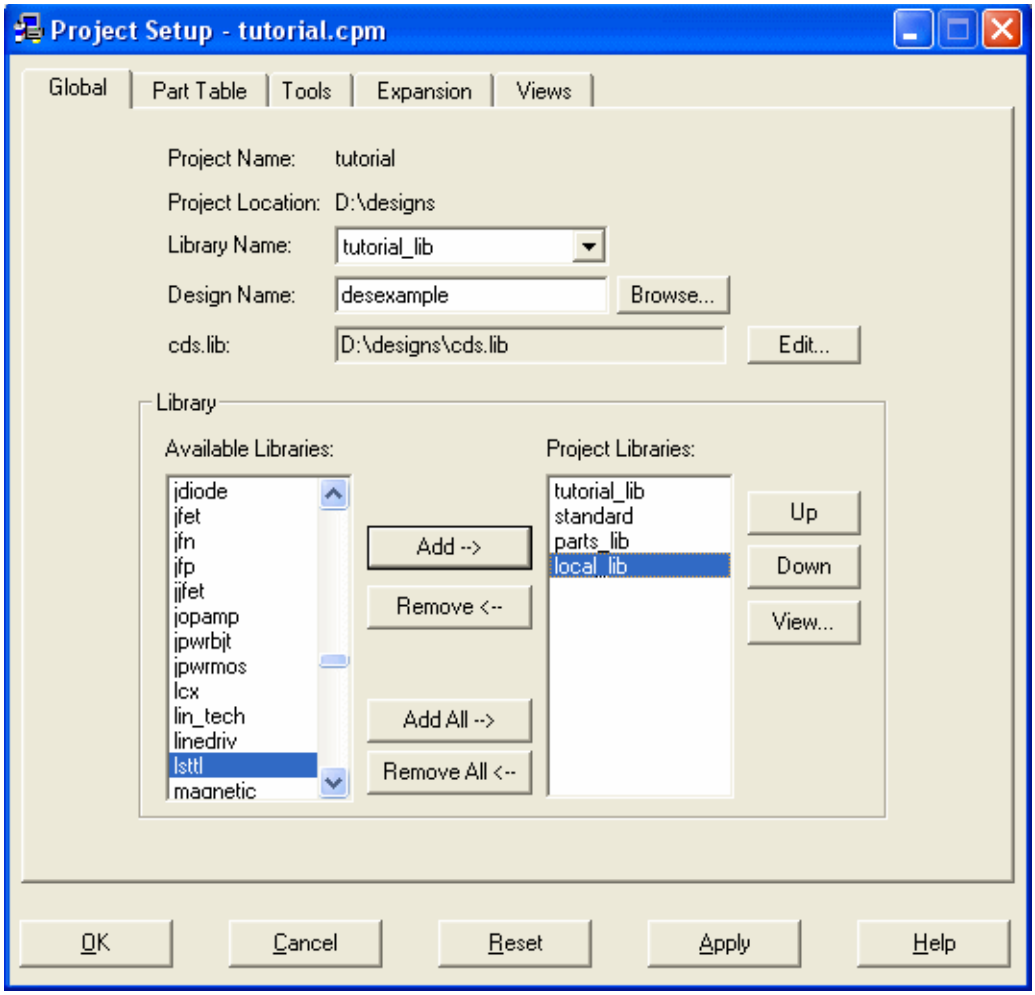


6. Click *Yes*.

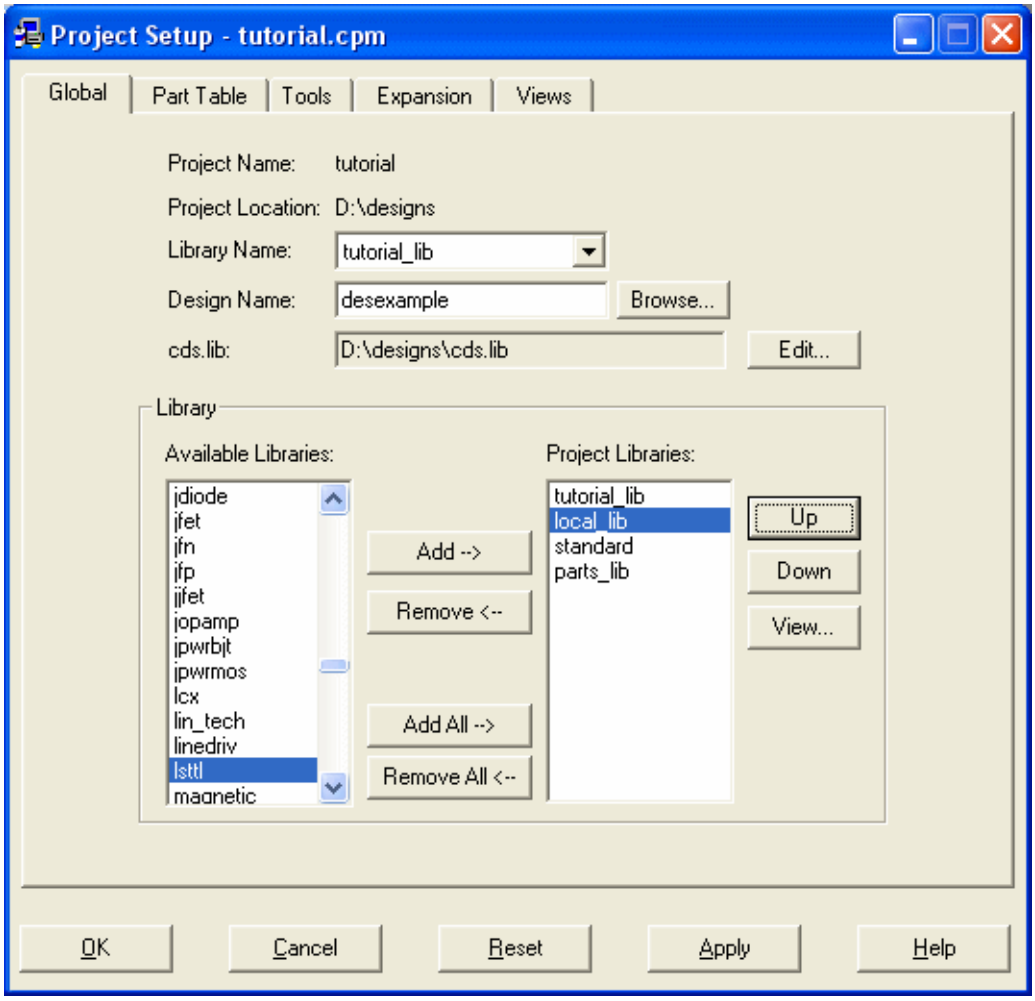
   Project Manager updates the *Available Libraries* list with the `local_lib` library.

7. Select *local_lib* from the *Available Libraries* list.

8. Click *Add*.



9. Select *local_lib* from the *Project Libraries* list.
10. Click *Up* until *local_lib* comes after *tutorial_lib* in the *Project Libraries* list.

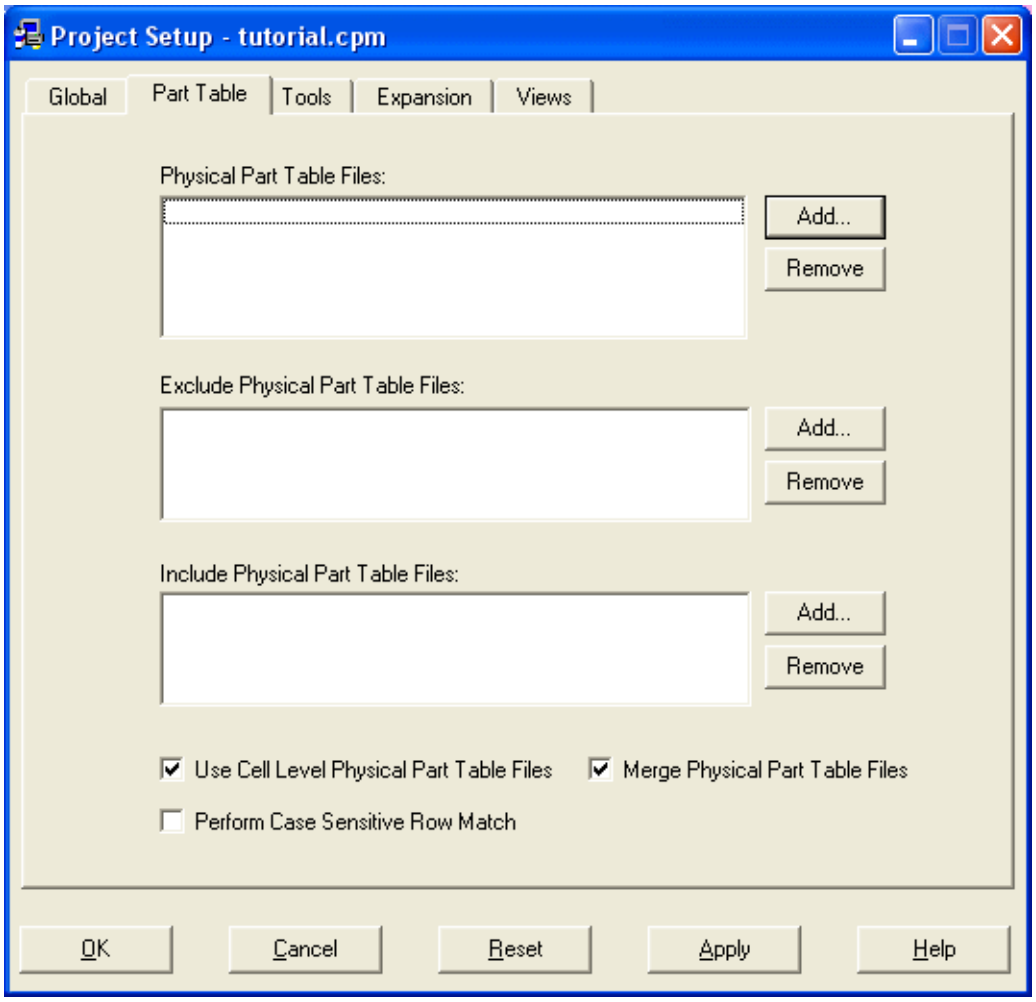


11. Select `lsttl` from the *Available Libraries* list.
12. Click *Add* to add `lsttl` to the *Project Libraries* list.

    Note: Some of the libraries listed in the above screen shot, such as `lsttl`, might not be available to you if you do not have the Cadence Libraries CD installed. In such a case, you may skip this step.

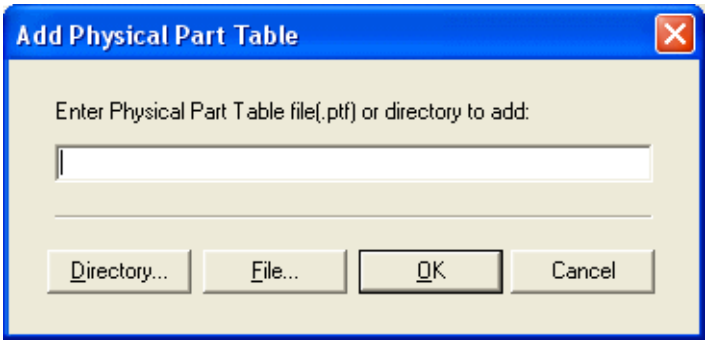
13. Click *Apply*.

14. Click the *Part Table* tab.



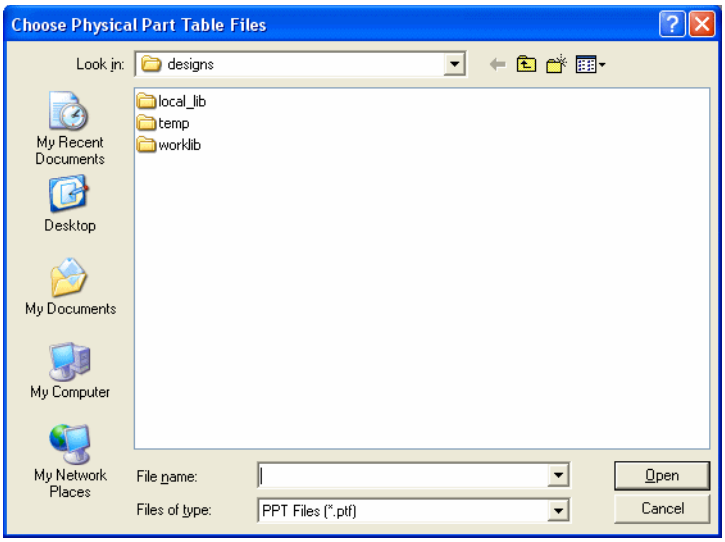
15. Click *Add* near the *Physical Part Table Files* field.

The Add Physical Part Table dialog box appears.



16. Click *File*.

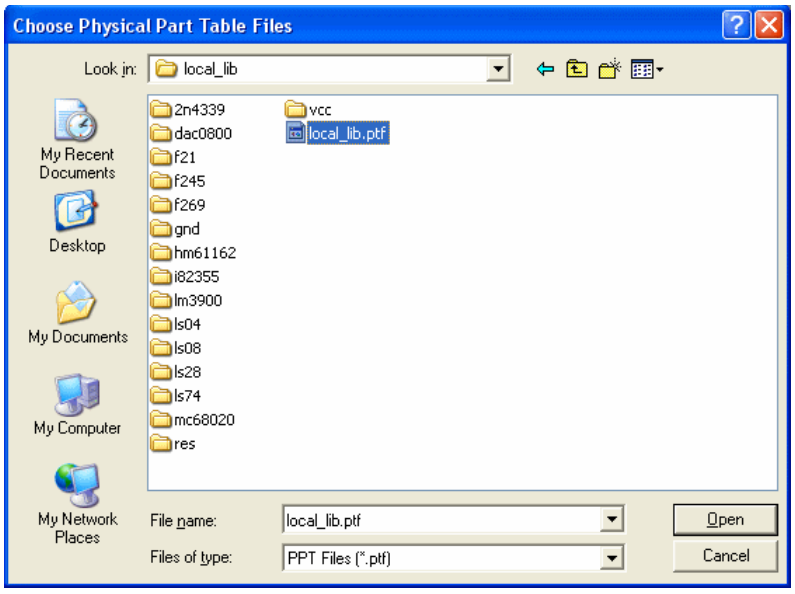
A file browser appears.



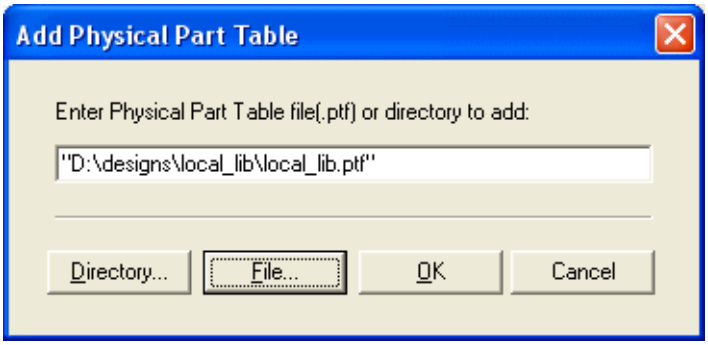
17. Open the `local_lib` folder.

18. Select the `local_lib.ptf` file.

19. Click *Open*.

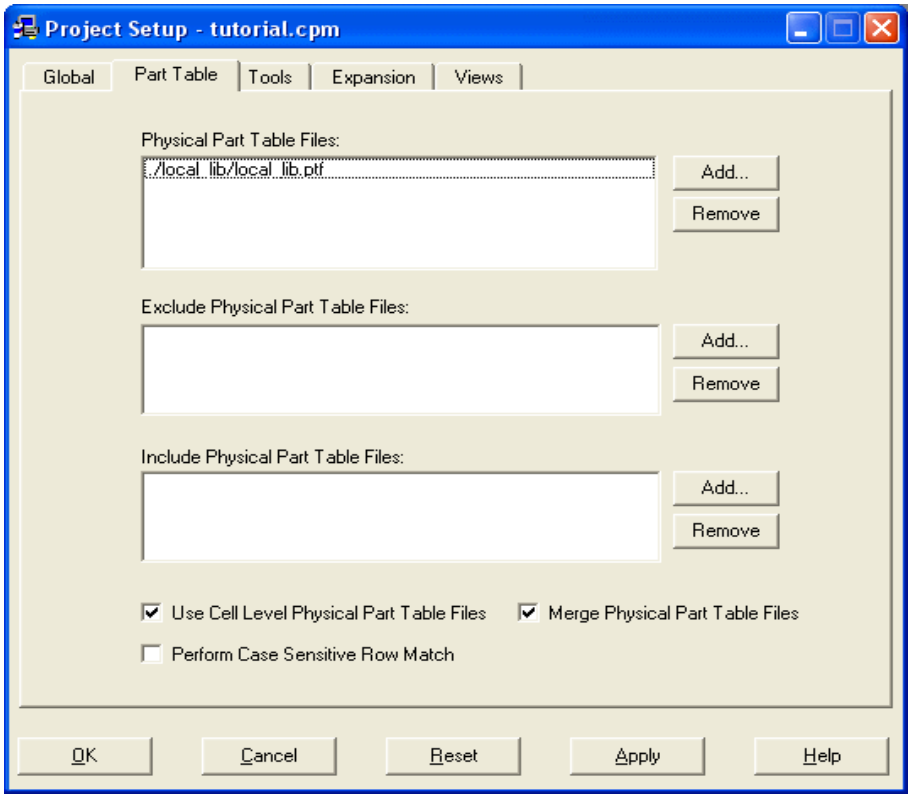


The *Add Physical Part Table* dialog box displays the path to the `local_lib.ptf` file.



20. Click *OK*.

The *Physical Part Table Files* field in the *Part Table* tab displays the path to the `local_lib.ptf` file.



21. Click *OK*.

The Project Setup dialog box is closed and you are returned to the Project Manager flow.

3

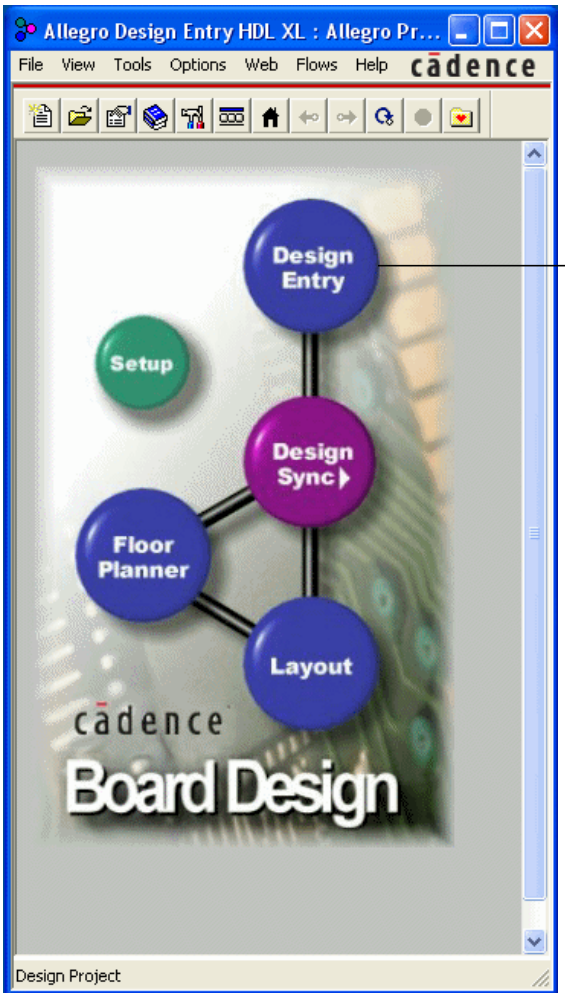
Creating a Schematic: Basics

Overview

This chapter contains the following information:

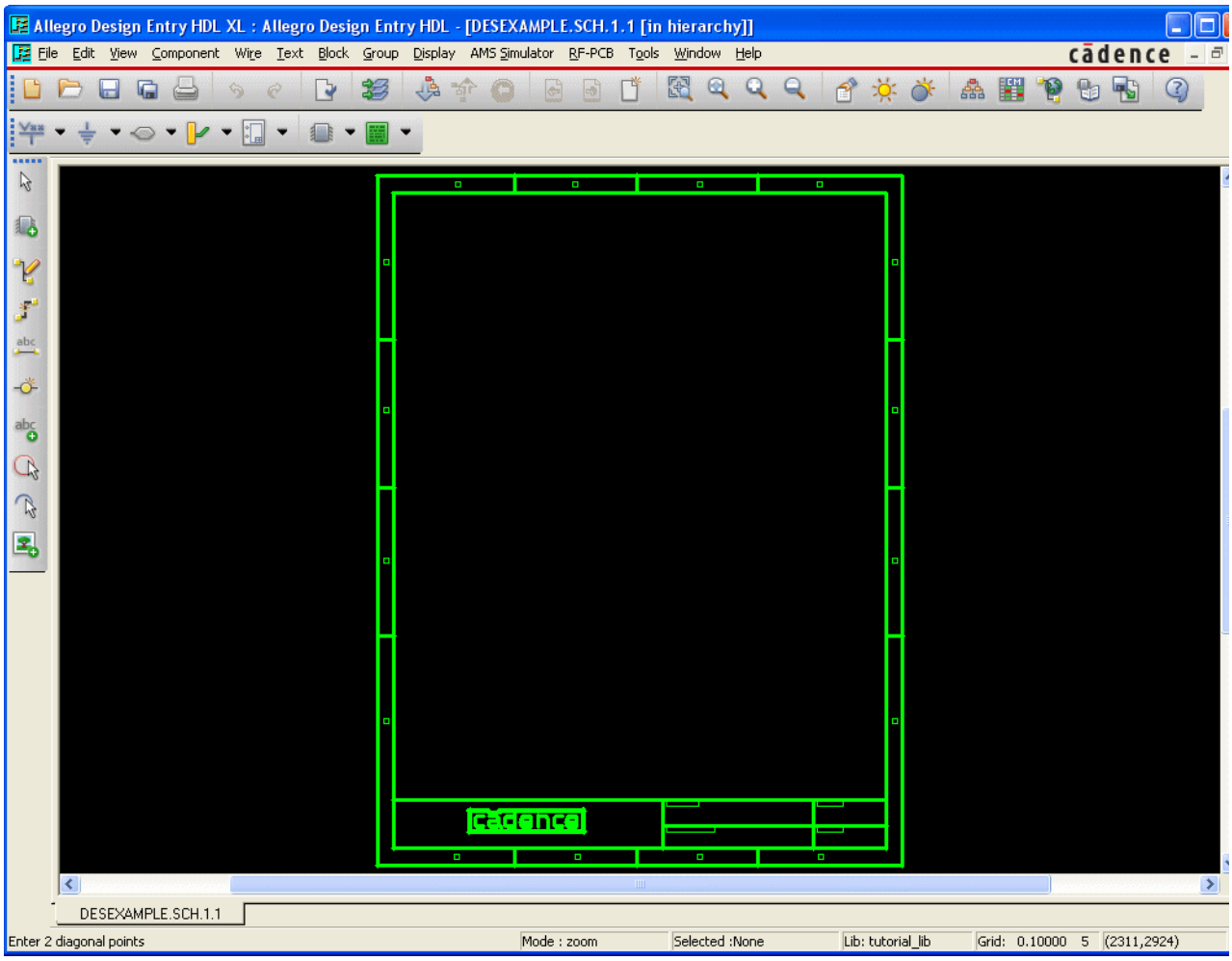
Starting Design Entry HDL

The first step in creating a logic design is starting Design Entry HDL. Using Design Entry HDL, you will place the components from project libraries and connect them to create a logic design. In Project Manager, click *Design Entry*.

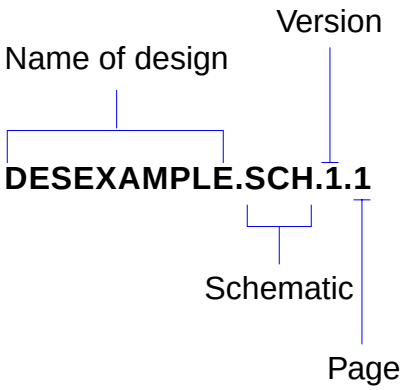


Click to start Design Entry HDL.

Allegro Design Entry HDL appears displaying the design name in the title bar.



The following figure explains the naming convention followed by Design Entry HDL.



The title bar also displays the term *in hierarchy* within square brackets. In hierarchy is one of the three modes in Design Entry HDL.

In Hierarchy Mode

When you open a design project in Design Entry HDL, the top-level drawing is displayed and the title bar displays the design name with the term *in hierarchy* within square brackets. This means that Design Entry HDL recognizes the design with all its pages and levels.

You can ascend or descend into the various pages and levels in this design by using *File – Edit Hierarchy – Ascend* and *File – Edit Hierarchy – Descend*, respectively.You can also use *File – Return* to return to the previous page you had viewed.

When you open a drawing that is not used in the design and is not in the hierarchy of the schematic, Design Entry HDL opens the drawing with just the design name in the title bar. You cannot use the *File – Return* feature in this case.

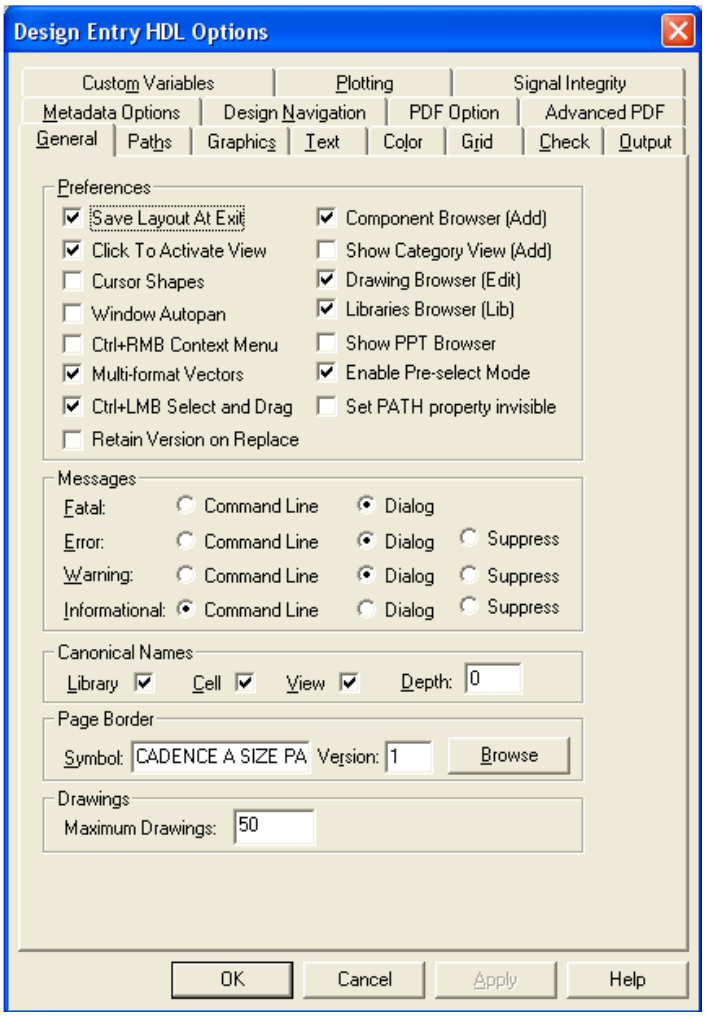
Setting the Pre-Select Use Model

The two use models supported by Design Entry HDL are pre-select and post-select. The post-select model is the default use model. To work in the pre-select model, you need to change the settings of Design Entry HDL. To set Design Entry HDL in the pre-select model, perform the following steps:

1. Choose *Tools – Options*.

   The Design Entry Options dialog box displays with the *General* tab selected.

   In the *Preferences* section, select the *Enable Pre-select Mode* check box.

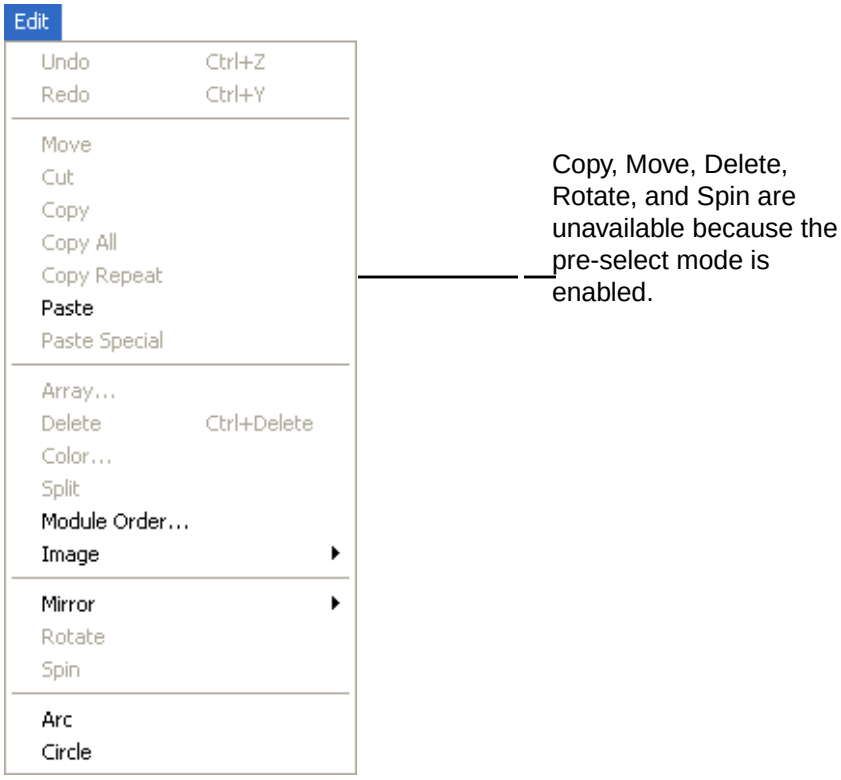


2. Click *OK* to save the settings and close the *Design Entry HDL Options* dialog box.

   The pre-select mode is enabled.

Note: You can verify whether the pre-select model is enabled or not by viewing the *Edit* pull-down menu. In the pre-select model, the command options such as *Copy*, *Move*, *Delete*, *Rotate*, and *Spin* are disabled by default. These options are enabled only after you select a schematic component.

Edit Pull-Down Menu in the Pre-select Mode



Note: The steps in this tutorial use the post-select mode.

3. Deselect the *Enable Pre-select Mode* check box in the *General* tab of the Design Entry Options dialog box.

Adding a Page Border

The first step while creating any design is to add a Page Border. You can have a design without page borders, but it is a good design practice to add page borders. Page borders are required when you cross reference a design. When you plot a schematic, it is often difficult to trace a signal or instances of a part. Cross Referencer traces the signals and parts in a schematic and annotates the location of each one in a file. Cross Referencer writes the page number and the location of the part or signal in relation to the page border.

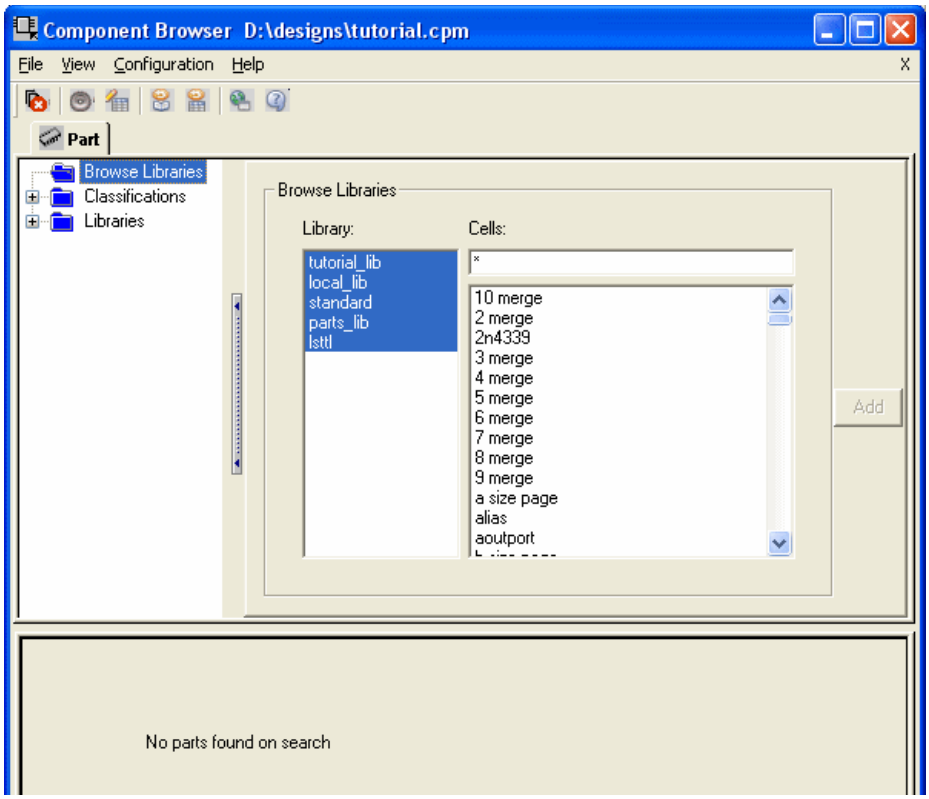
There are two ways in which you can add a page border. The first method is adding the page border manually on each page and the second method is to set Design Entry HDL options such that the page border is added as soon as a new page is created.

Adding a Page Border Manually

Design Entry HDL treats page borders as components.

1. To select and place a page border, choose *Component – Add*.

   Component Browser appears as shown in the following figure.



2. Click the *Browse Libraries* node and then choose *standard* in the Library field.

   The components in the Standard library appear in the Cells list.

3. Choose *cadence a size page* from the *Cells* list.
4. Click *Add*.
5. Click in the Design Window.

   Design Entry HDL displays the page border.

6. Choose *File – Exit* to exit Component Browser.

Adding a Default Page Border

You can set options in Design Entry HDL to add a page border by default, whenever a new page is added to the design.

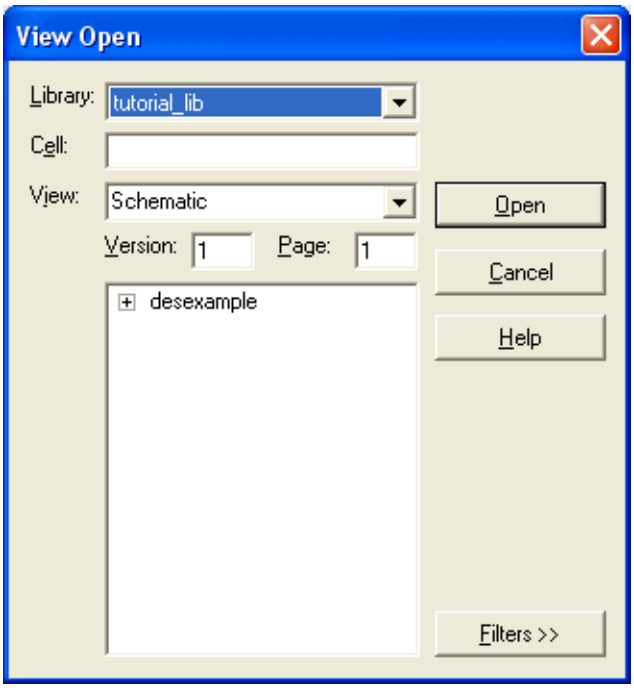
1. Choose *Tools – Options*.

   The Design Entry Options dialog box appears with the *General* tab selected.

2. In the *Page Border* section specify the name and version of the page border symbol that is to be added to all the pages.

   To specify the symbol name, click *Browse*.

The View Open dialog box is displayed.



3. Select the `Standard` library.

   The list of components available in the *Standard* library appears.

4. From the list, select a page border.

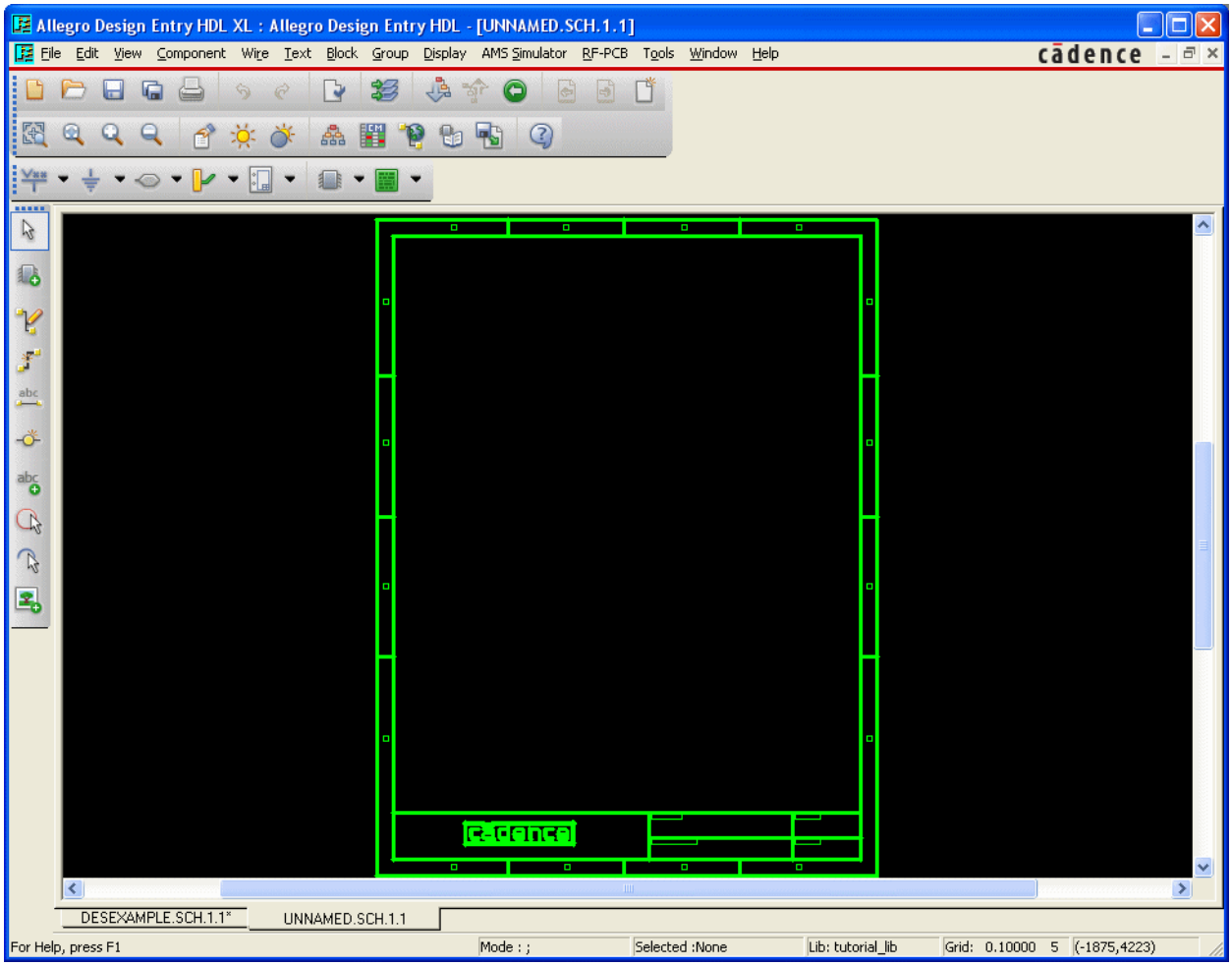
   For this tutorial, select *cadence a size page* and click *Open*.

   The Design Entry Options dialog box reappears with the *Symbol* and *Version* of the page border added.

5. Click *OK* to save the settings.

6. Choose *File – New* in the Design Entry HDL design window.

A new design named UNNAMED.SCH.1.1 appears with the page border added. All new designs or the pages added to a design will now have the defined page border.



7. To close the design UNNAMED.SCH.1.1 and return to the design DESEXAMPLE.SCH.1.1, choose *File – Close*.

Adding Text (Notes)

You can also add additional details to the schematic, such as the following:

- Title (name of the design)
- Engineer (name of the Engineer who created the design)
- Date (date of creation)
- Page (page number)

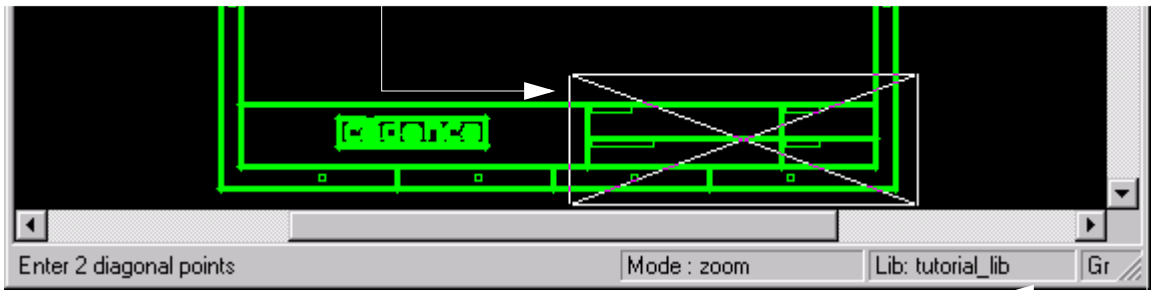
To add text on the page border, you need to zoom into the area where you can enter text.

To zoom into an area

1. Click the *Zoom Points* icon  on the Standard toolbar.
2. Click on the design window and drag to form a rectangle for zooming into an area in the page border.

1. Click and leave left mouse button

2. Drag to draw rectangle for selecting the area to zoom.
3. Click to end drawing the rectangle and zoom into the selected area.



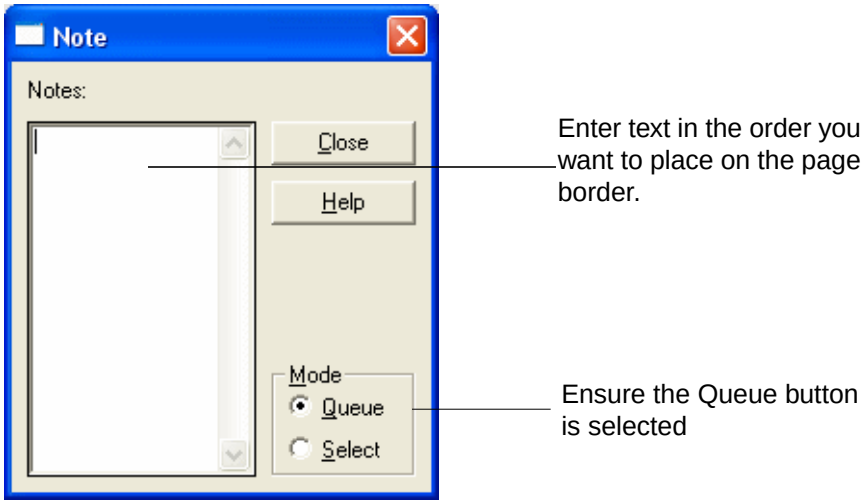
3. Once the area is zoomed into, click the design window again.

   Design Entry HDL zooms into the area.

To add text (notes) in the page border

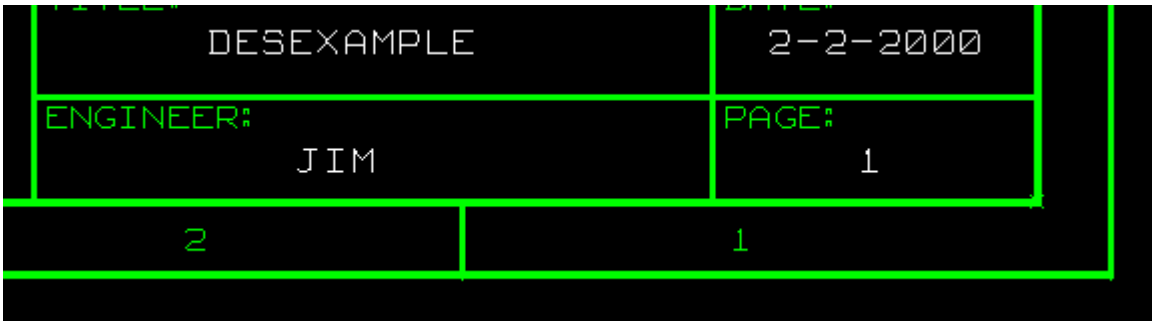
1. Choose *Text – Note.*

   The Note dialog box appears.



2. Enter the following text in the Notes field:
   - DESEXAMPLE
   - JIM
   - 2-2-2000
   - 1
3. Click the following fields in the page border in the following order:
   a. TITLE
   b. ENGINEER
   c. DATE
   d. PAGE

   Design Entry HDL adds notes in the order you enter them in the Notes field, at the places you click in the page border.



4. Click *Close* in the Note dialog box.
5. Click the *Zoom Fit* button on the Standard toolbar  to view the entire page.

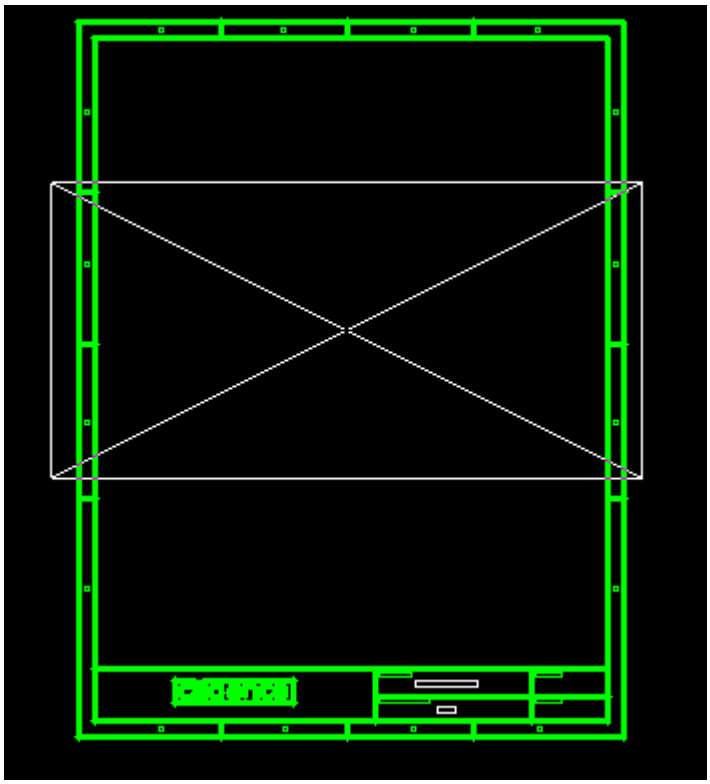
   Design Entry HDL fits the entire page in the design window.

Choosing and Adding Components

Creating a project using Design Entry HDL involves different steps, such as adding components, connecting the components using wires, and adding input/output ports.

The components are stored in different libraries. Use Component Browser to choose components from project libraries and place them on the Design Entry HDL design window.

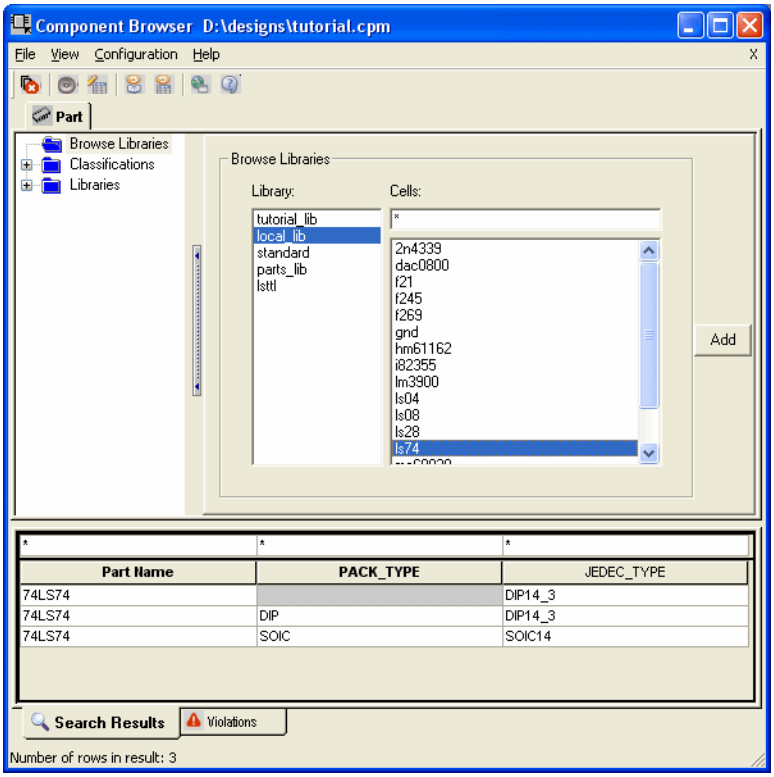
1. Click the Zoom by Points button and zoom into the area shown below.



Design Entry HDL zooms into the selected area.

2. Choose *Component – Add* to start the procedure of adding components.

The Component Browser dialog box is displayed.



3. Select `local_lib` in the *Library* field.

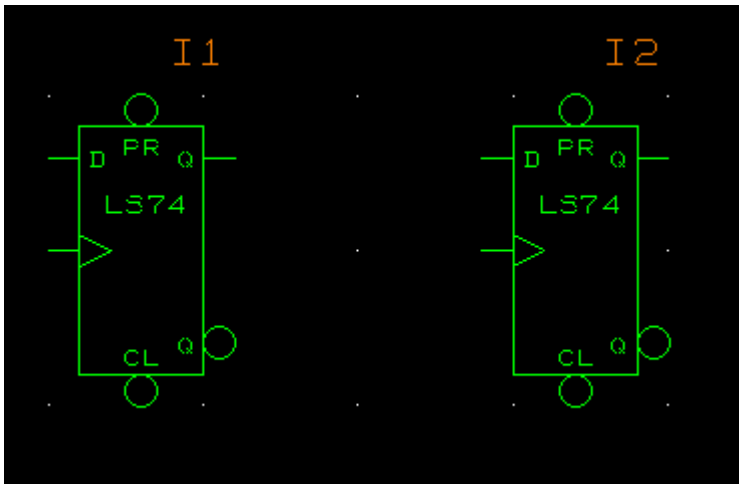
   The components of the *local_lib* library appear in the Cells list.

4. Select LS74 from the *Cells* list and click *Add*.

5. Click in the Design Window.

   The LS74 component is placed on the schematic.

6. Place another instance of `LS74` adjacent to the first instance of `LS74`.



7. Choose *File – Exit* to close the Component Browser dialog box.

   For each instance of a component you place, Design Entry HDL automatically assigns a PATH property. This property has a unique value that helps identify the instance, for example, `I1, I2, I3...In`.

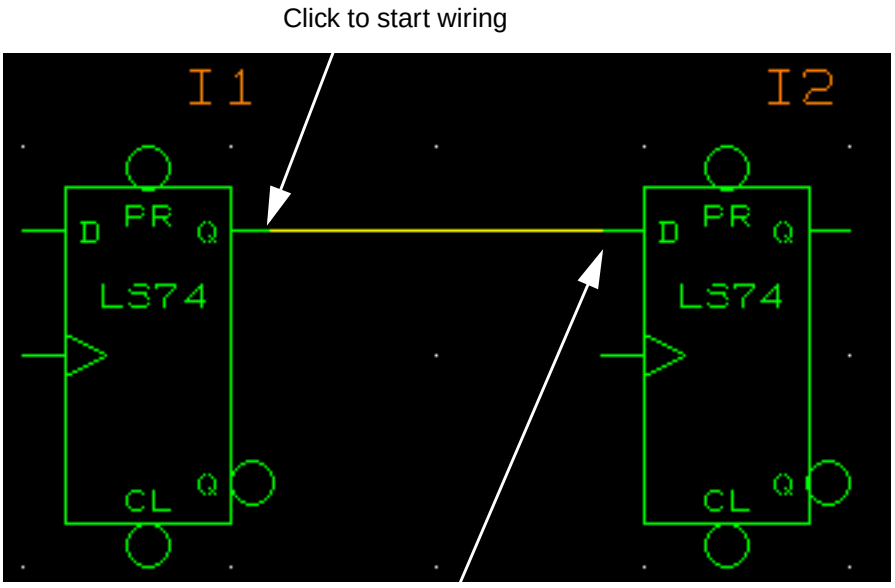
   In the previous example, the two instances of the component `LS74`, are identified as `I1` and `I2`.

Connecting Parts

After placing the components on the Design Entry HDL design window, you need to connect the components by using wires.

1. Choose *Wire – Draw.*
2. Click first at the tip of pin `Q` of `I1` and then at the tip of pin `D` of `I2` to connect the components.

Design Entry HDL connects pin Q of I1 and pin D of I2 as shown in the following figure.



Note: While drawing wires, start the wire from the tip of the pin and do not cover the pin completely.

Place the LS04 component between the pin Q of I1 and pin D of I2.

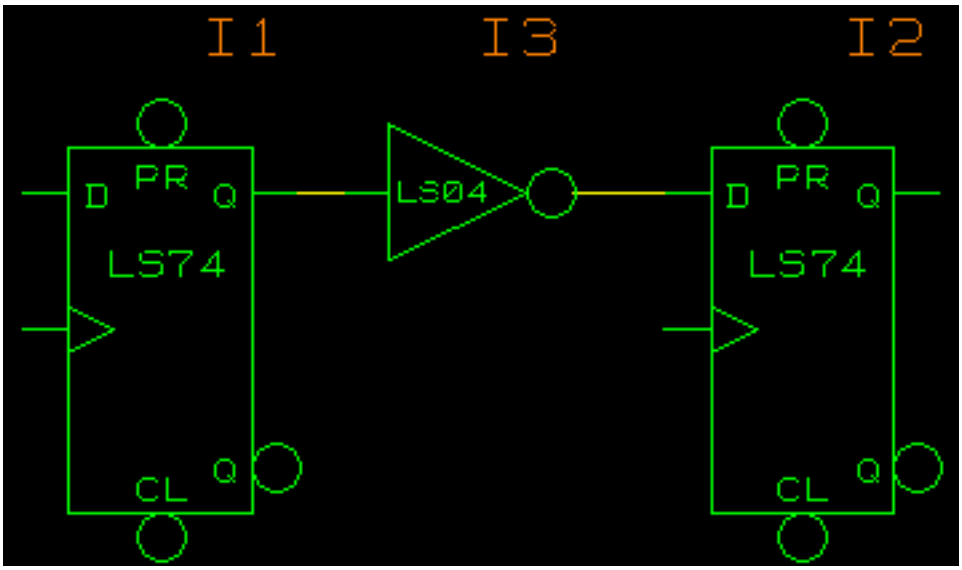
3. Choose *Component – Add*.

   Component Browser appears.

4. Choose LS04 from the Cells list and place on the wire connecting I1 and I2.

5. Close Component Browser.

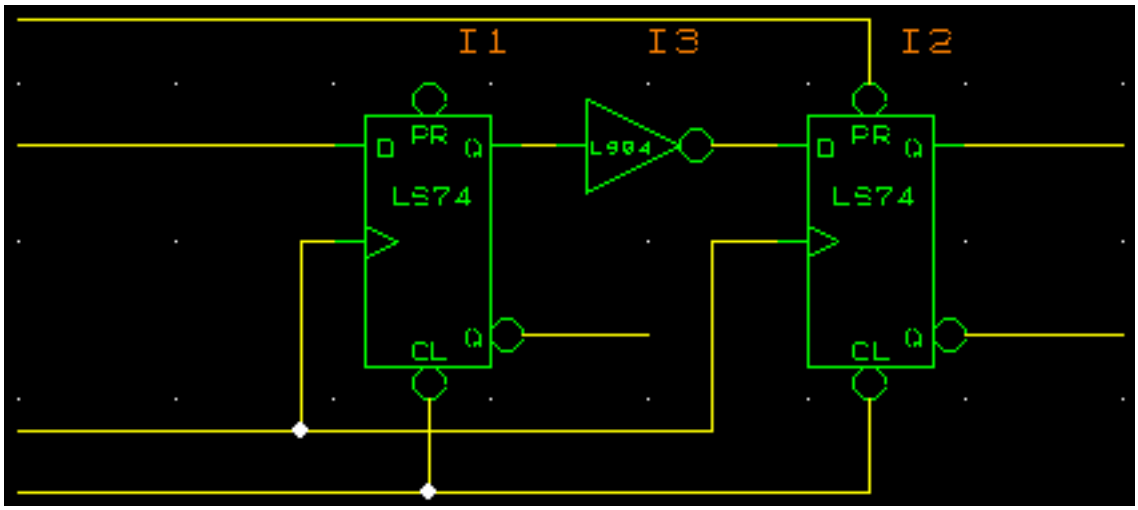
LS04 is connected with I1 and I2 as shown in the figure below.



6. Choose *File – Save* to save the schematic.

Design Entry HDL saves the schematic without any errors.

7. Add more wires to the components as shown in the following figure.



Note: Double-click to terminate a wire at a location that is not a pin or another wire.

8. Right-click and select *Done*.

Naming Wires

Design Entry HDL supports connection by name. If two signals on the same or different pages of the same design have the same name, Design Entry HDL considers them to be the same signals. Design Entry HDL does not require the use of off-page connectors for signals spanning multiple pages.

1. Choose *Wire – Signal Name*.

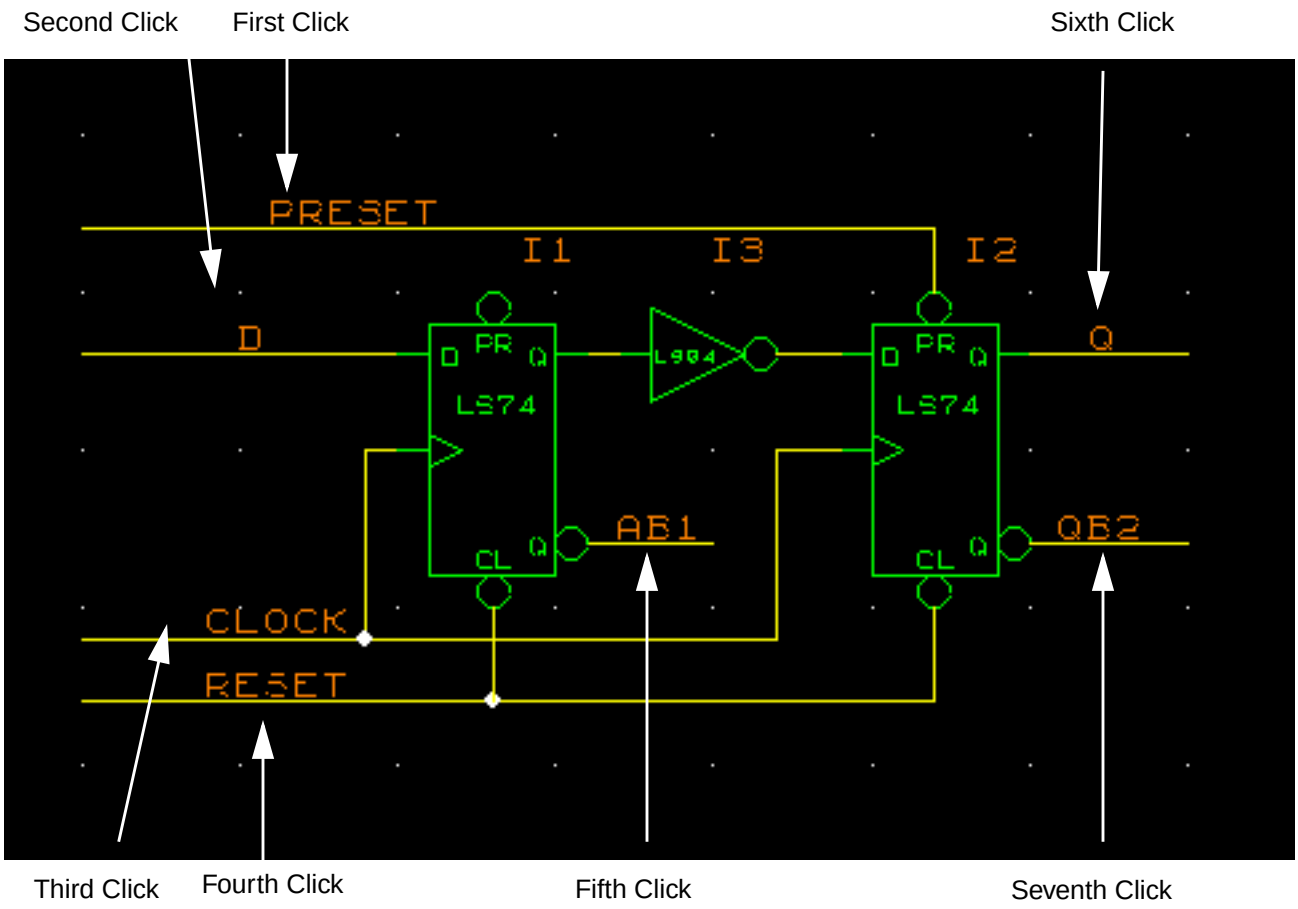
   The Signal Name dialog box appears.

2. Enter the following text in the given sequence in the *Signal Names* field.

   - PRESET
   - D
   - CLOCK
   - RESET
   - AB1
   - Q
   - QB2

3. Ensure the *Queue* option is selected

4. Click the wires one after another to name each one of them as shown in the following figure.



Adding Ports

Cadence supplies input and output ports in the standard library. You can use *Component Browser* to select and place a port in the schematic.

1. Choose *Component – Add.*

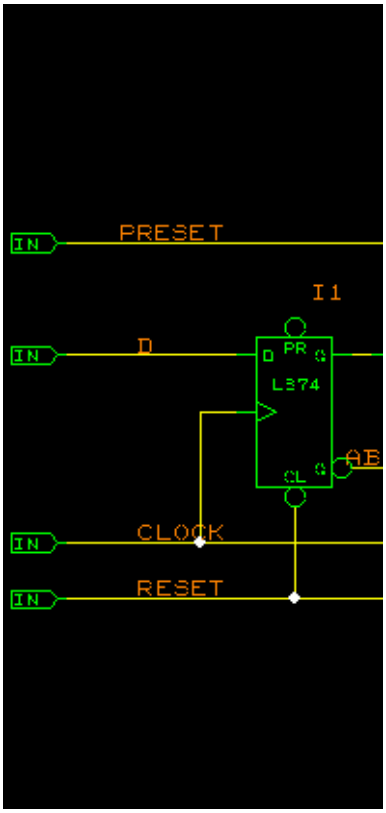
   Component Browser appears.

2. Choose `Standard` as the *Library*.
3. Choose `INPORT` from the *Cells* list and click *Add*.
4. Click at the tip of the wire named `PRESET` to place `INPORT`.

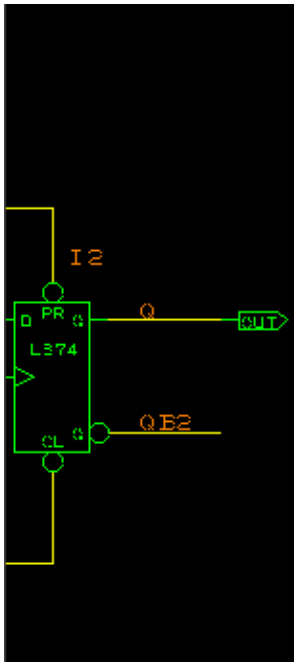
This defines PRESET as an input port.

5. Click the schematic to instantiate INPORT again.
6. Click again at the tip of wire D to place INPORT.

   Similarly, instantiate and place INPORT on wires as shown in the figure below.



7. In Component Browser, select OUTPORT from the *Cells* list and click at the tip of the wire named Q to place OUTPORT as shown in the following figure.



8. Close the Component Browser dialog box.

Adding Power and Ground

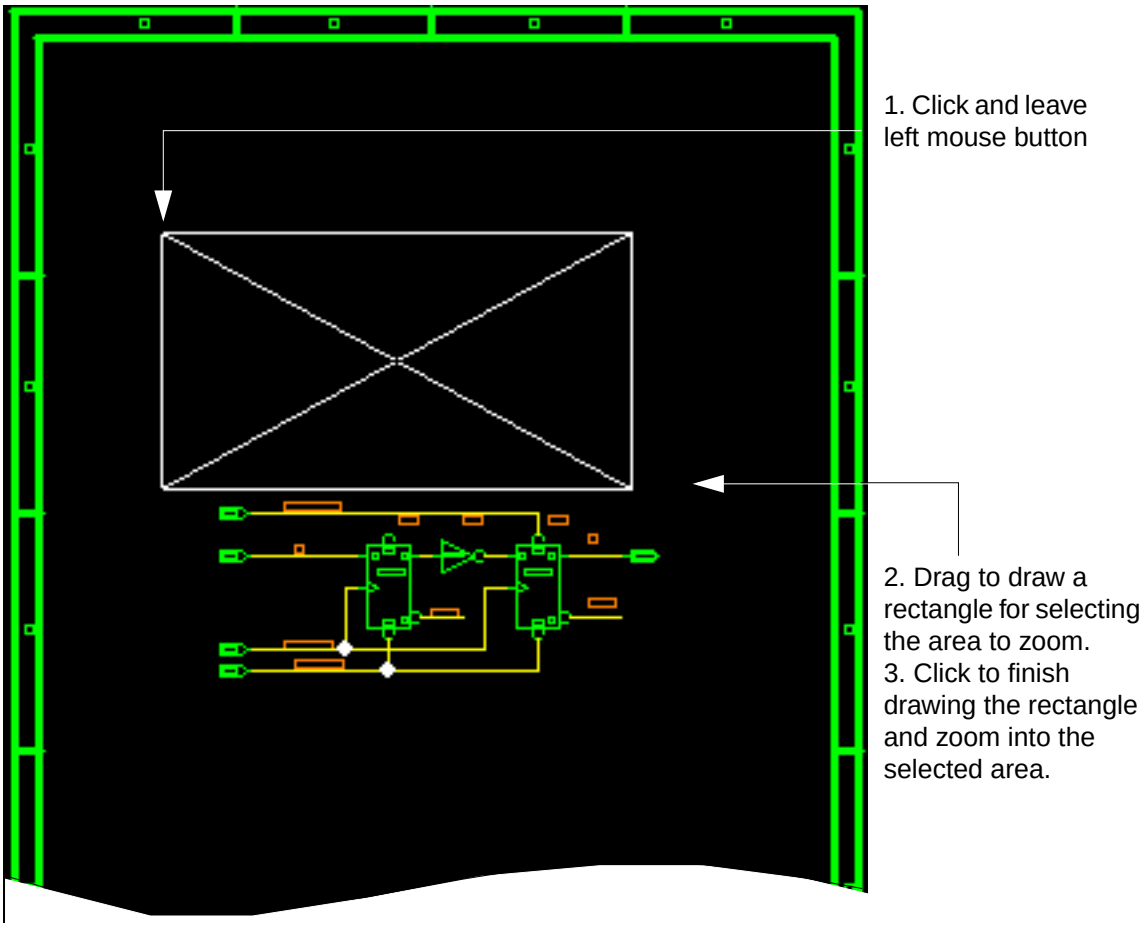
The next step is to add power to wire AB1 and ground to wire QB2. The required power and ground pins are available in the `local_lib` library.

1. Click the Zoom Fit button on the Standard toolbar.

   Design Entry HDL fits the schematic page in the design window.

2. Click the Zoom Points button on the Standard toolbar.

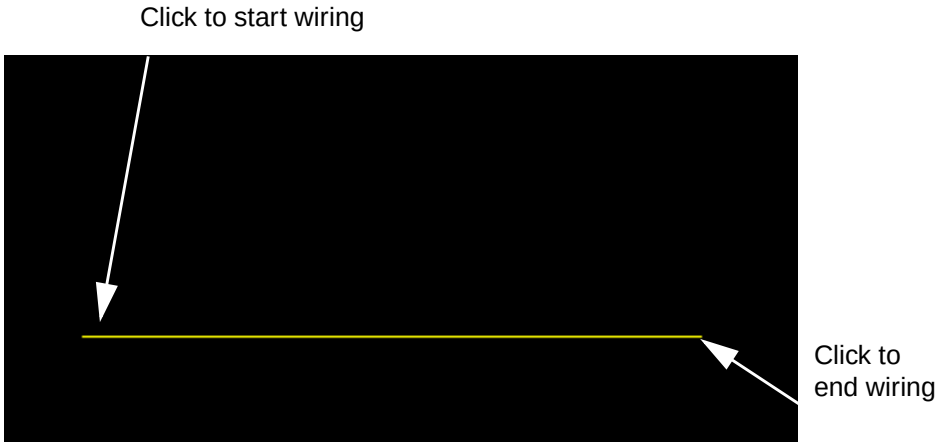
3. Select the area to zoom in as shown in the following figure.



Design Entry HDL zooms into the selected area.

4. Choose *Wire – Draw.*

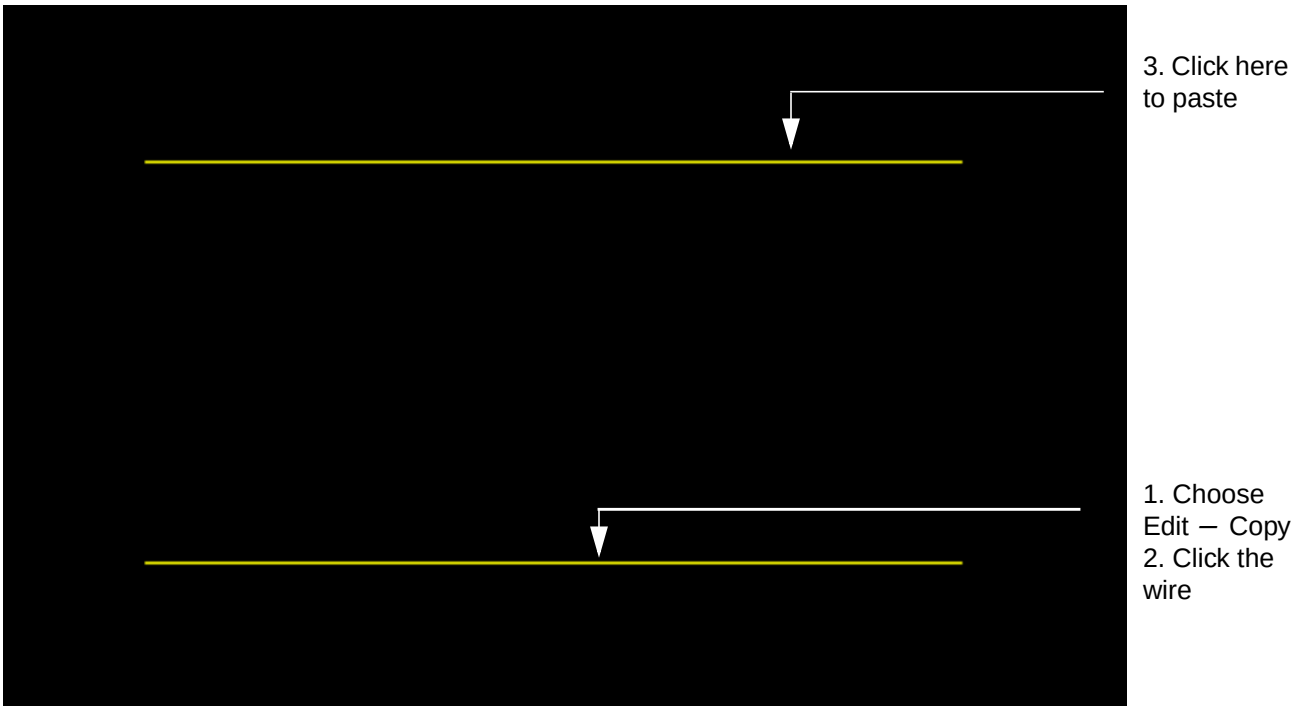
5. Draw a horizontal wire as shown in the following figure.



6. Right-click and choose *Done*.

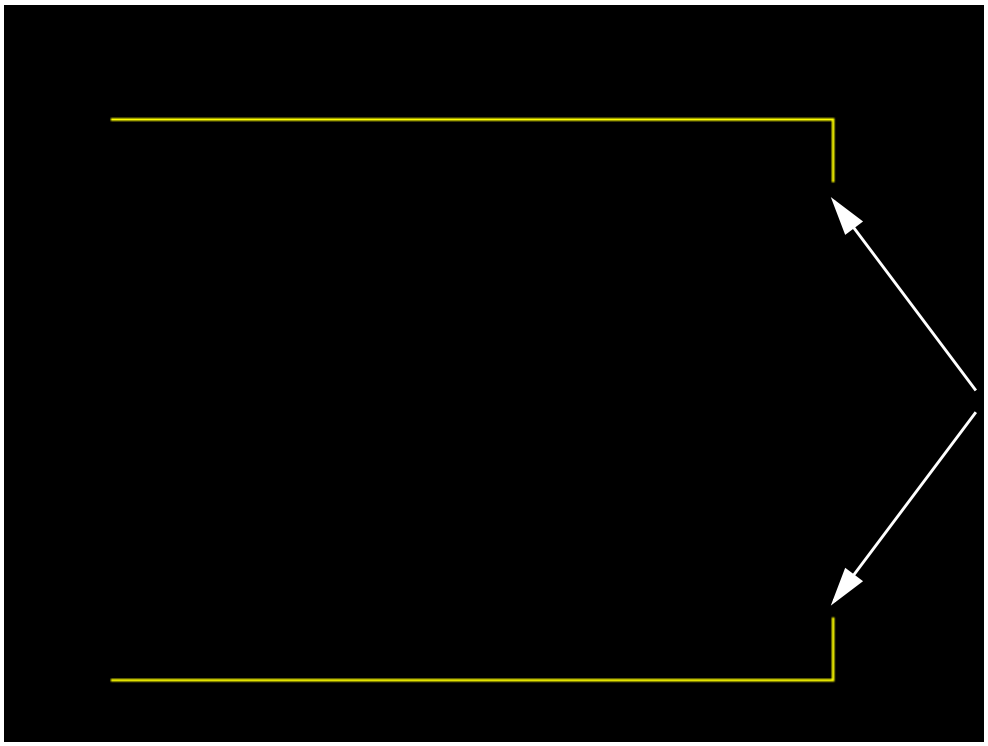
7. Choose *Edit – Copy*.

8. Click the wire and click above to paste as shown in the following figure.



9. Right-click and choose *Done*.

10. Extend the wires as shown in the following figure.

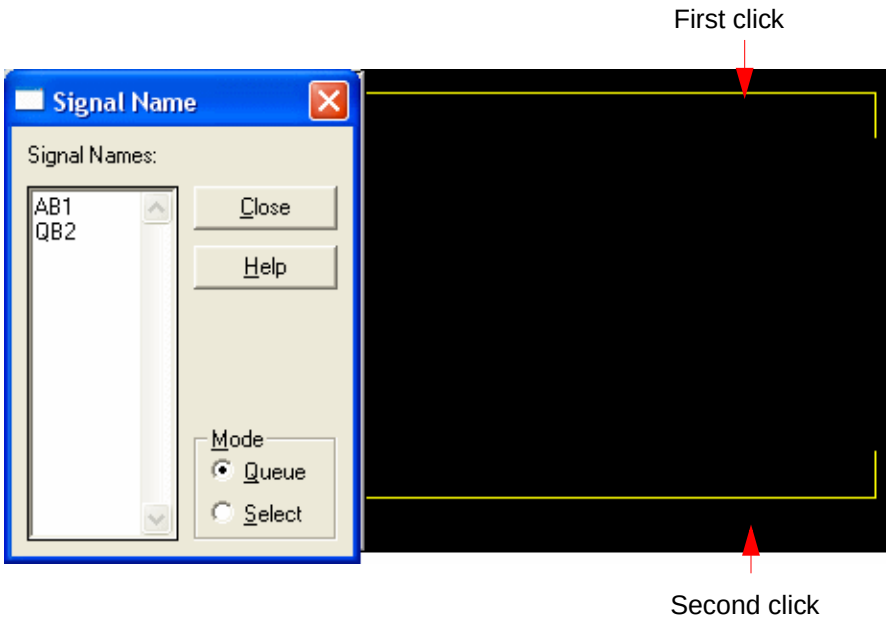


11. Right-click and choose *Done*.

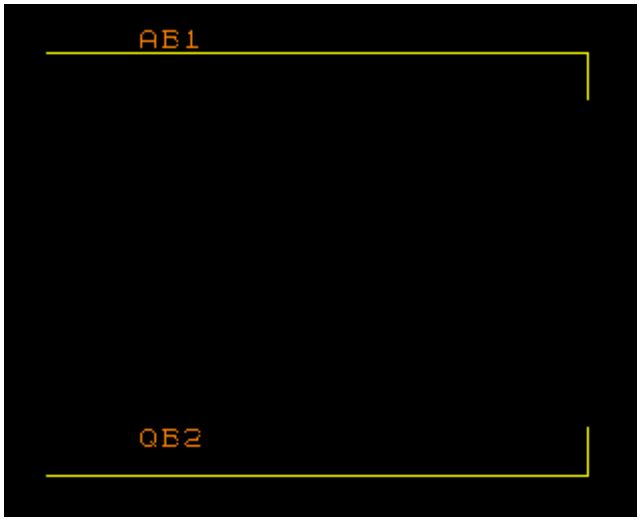
12. Choose *Wire – Signal Name*.

The Signal Name dialog box is displayed.

13. Enter AB1 and QB2 as signal names and click the wires as shown in the following figure.



Design Entry HDL names the wires as shown below.



14. Click *Close* in the Signal Name dialog box.

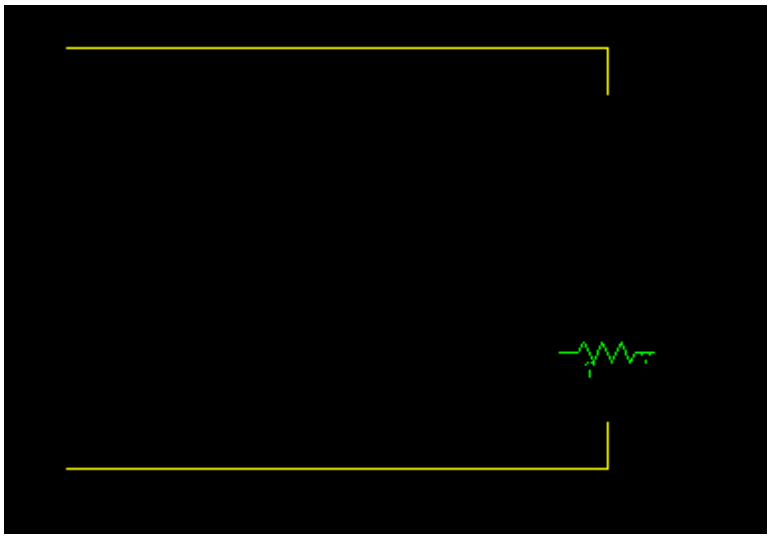
15. Choose *Component – Add*.

The Component Browser dialog box is displayed.

16. Choose `local_lib` as the library.

17. Choose RES from the *Cells* list.

18. Click the Design Window to place the resistor as shown in the figure below.



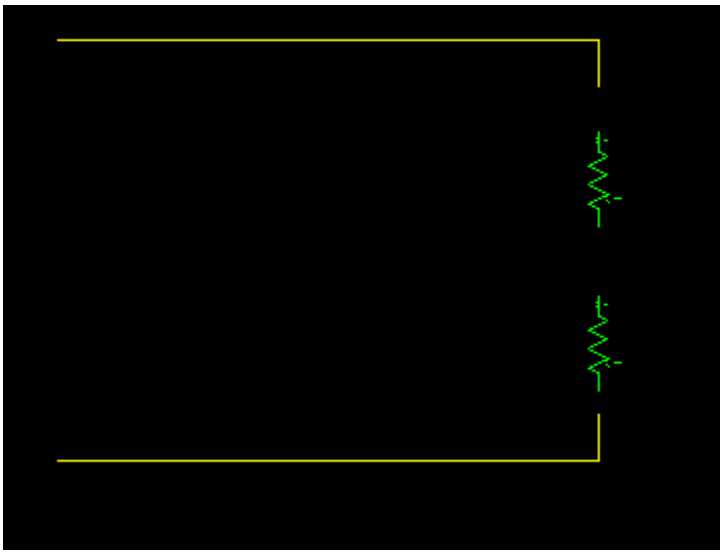
19. Choose *Edit – Rotate* and click the resistor.

Design Entry HDL rotates the resistor as shown below.

20. Right-click and choose *Done*.

21. Choose *Edit – Copy*.

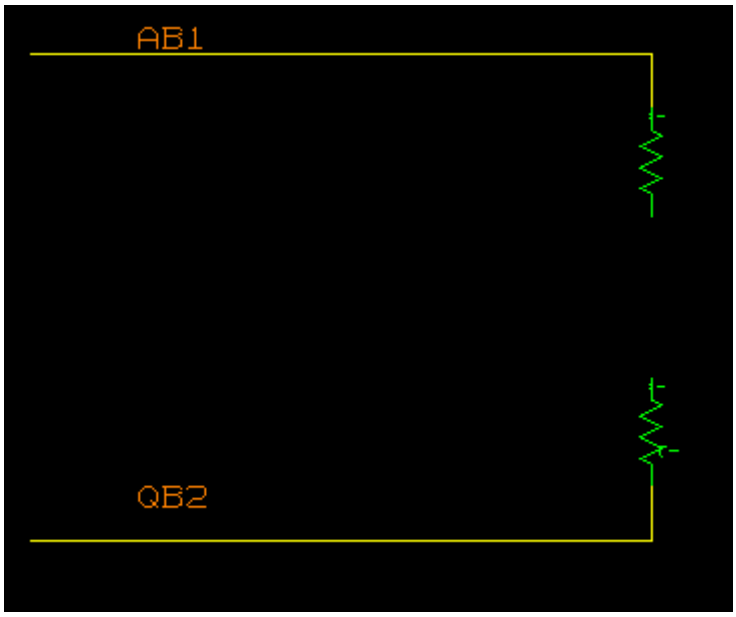
22. Click RES and click again to paste a copy of RES as shown in the following figure.



23. Choose *Edit – Move*.

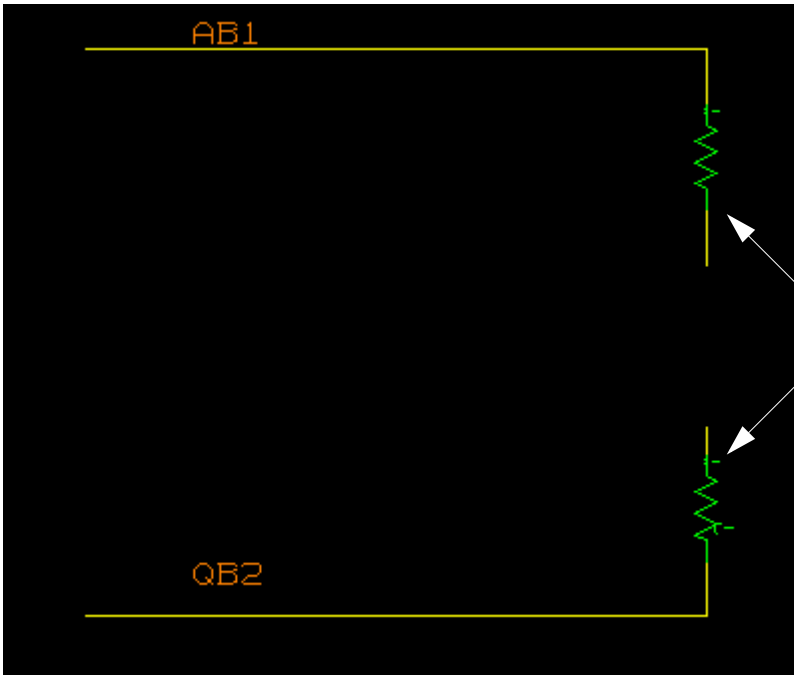
24. Click a resistor and connect it to the wire.

25. Click the second resistor to connect the second wire as shown in the following figure.



26. Choose *Wire – Draw*.

27. Draw wires at the ends of the resistors as shown in the following figure.



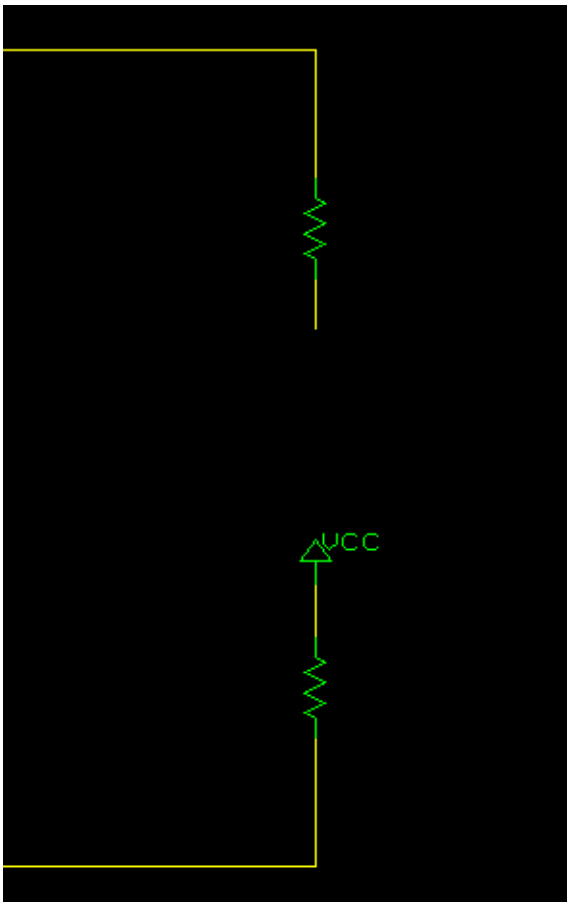
28. Choose *Component – Add*.

Component Browser is displayed.

29. Choose *local_lib* as the *library*.

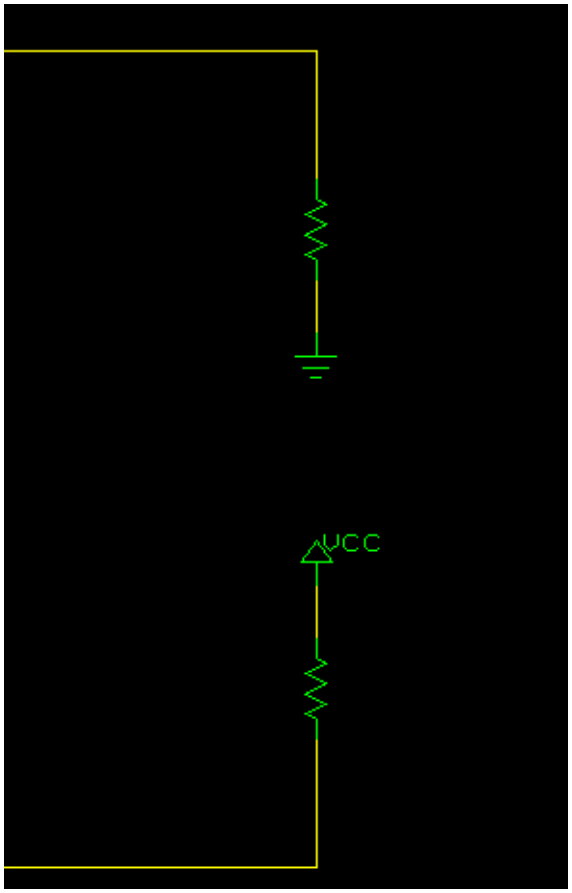
30. Choose *VCC* from the Cells list and then click *Add*.

31. Click in the Design Window to place VCC as shown in the following figure.



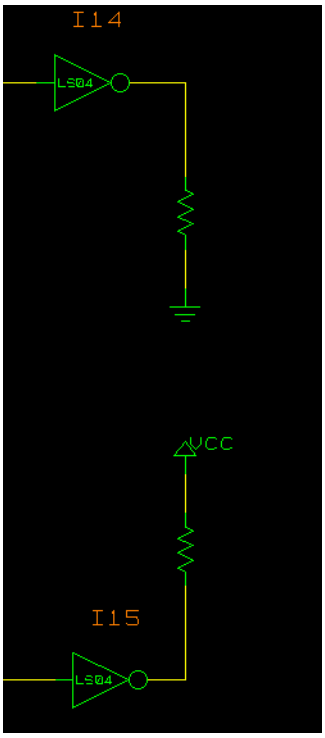
32. Choose *GND* from the Cells list and click *Add*.

33. Click in the Design Window to place GND as shown in the following figure.



34. Choose *LS04* from the Cells list.

35. Place LS04 on AB1 and QB2 as shown in the following figure.



36. Choose the Component Browser.

37. Right-click and choose *Done*.

38. Click the Zoom Fit button on the Standard toolbar.

Design Entry HDL fits the page on the Design Window.

Video

See the multimedia demonstration titled, *Creating a Schematic* for an example of the design project creation. The demonstration is available on SourceLink. The instructions to access this and other demonstrations on SourceLink are available on the *Legacy Demos* page of the Allegro Design Entry HDL Help System page. To launch the Help System page, choose *Help – Documentation* in Design Entry HDL, and click the *Demos* tab.

Saving the Schematic

To save the design, choose *File – Save*.

Design Entry HDL provides the option for writing the netlist when you save a schematic design. To access this option, choose *Tools – Options*.

In the Design Entry Options dialog box, select the *Output* tab.

A Verilog netlist is created if the *Create Netlist* check box is selected. By default, this option is selected. If you do not want to create the netlist, deselect the *Create Netlist* check box.

If the *Create Netlist* check box is selected, you can also create a VHDL netlist along with the Verilog netlist. To create the VHDL netlist, select the *VHDL* check box.

If a netlist is created after the design is saved, Design Entry HDL displays the following text in the Console Command window.

```
...HDL Written
```

Viewing the Verilog Description

1. Choose *File – Open*.

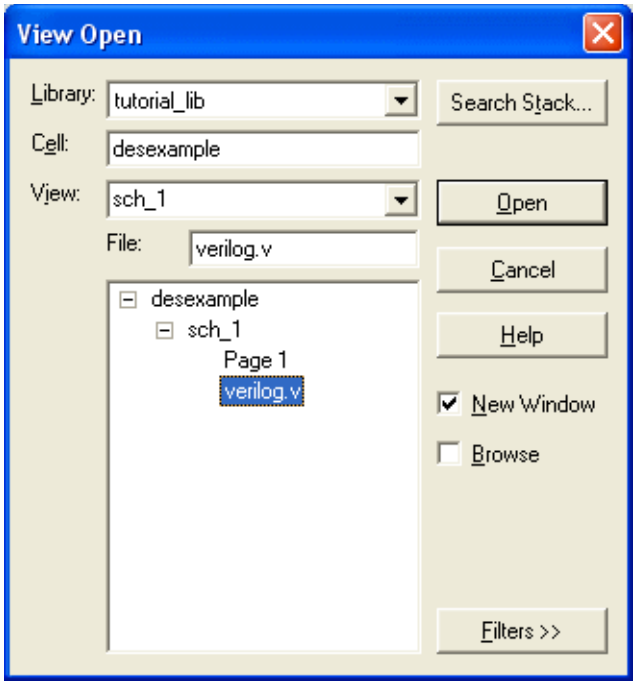
   The *View Open* dialog box appears.

2. Choose `tutorial_lib` as the library.

3. In the tree view, double-click *DESEXAMPLE*.

4. Double-click *sch_1*.

5. Select `verilog.v`.



6. Click *Open*.

   Design Entry HDL opens the Verilog description of DESEXAMPLE in the default text editor.

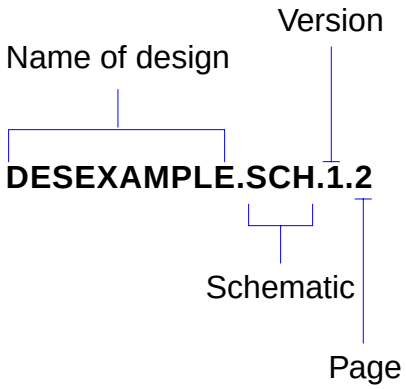
Adding Pages to the Schematic

While creating a design, it is not always possible to fit the entire design in a single page. You can have a schematic design extending multiple pages.

1. To add a new page to the schematic, choose *File – Edit Page/Symbol – Add New Page*.

   A new page is added and displayed. The title bar shows displays [DESEXAMPLE.SCH.1.2].

   The following figure explains the naming convention followed by Design Entry HDL.

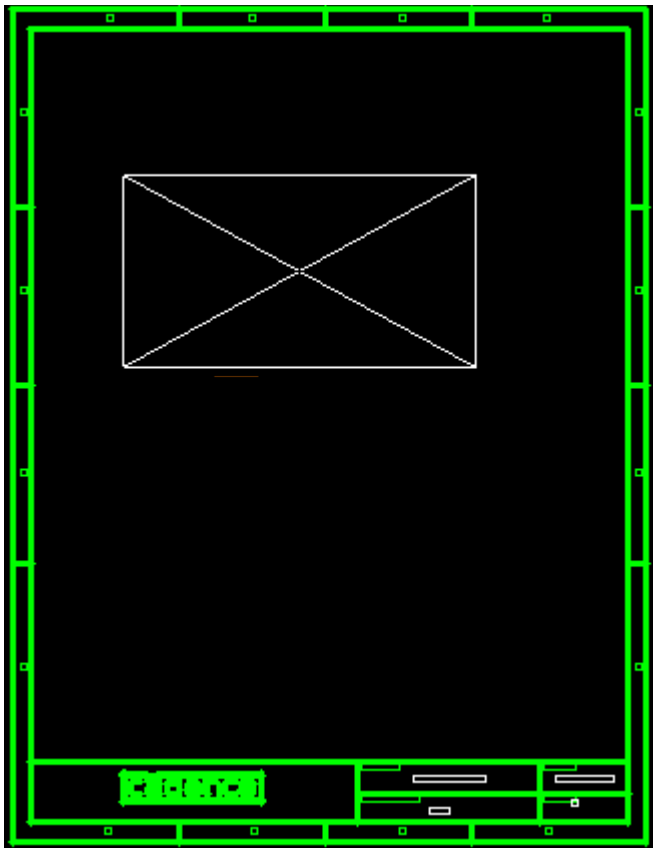


2. The new page appears with the page border added.

   Add text on the page border to specify the name of the engineer, title of the design, date of creation, and the page number. Specify the page number as 2.

3. Click the Zoom Points button on the Standard toolbar.

4. Select the area to zoom in as shown in the following figure.



Design Entry HDL zooms into the selected area.

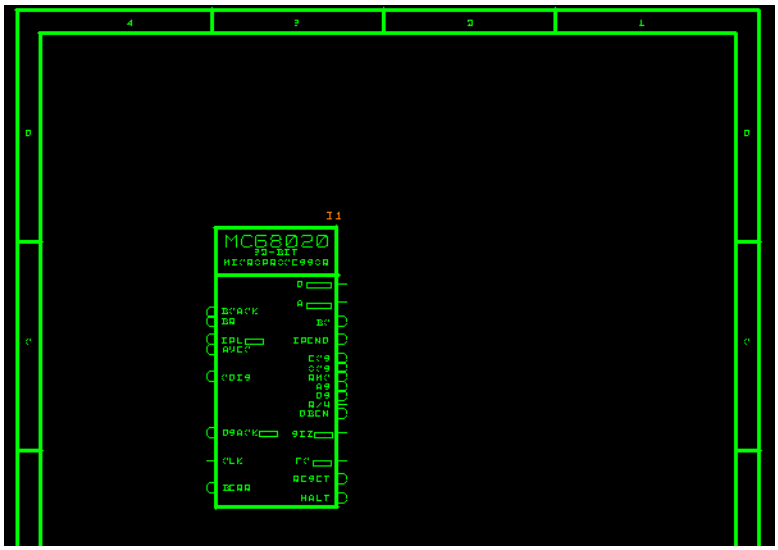
Add a component, `MC68020`, to the schematic page.

5. Choose *Component – Add*.

Component Browser appears.

6. Select `local_lib` from the *Library* list.
7. Select `MC68020` from the *Cells* list and click *Add*.

8. Click the Design Window to place MC68020.

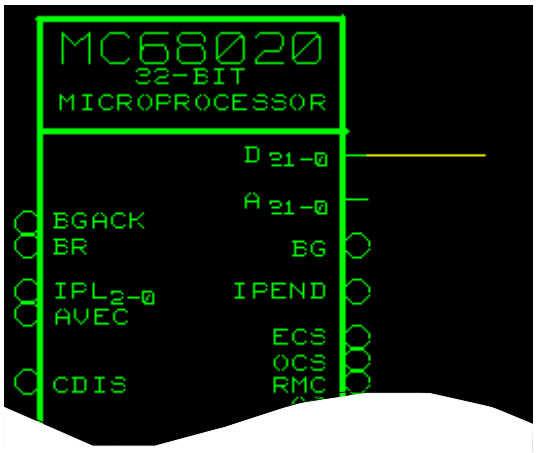


9. Close Component Browser.

Creating Buses

Creating buses is similar to creating wires, but the naming convention used is slightly different. The convention used is name<n-1..0> where n represents the bus size in bits. A 16-bit bus named DATA is represented as DATA<15..0>, and a 32-bit bus with the same name is represented as DATA<31..0>.

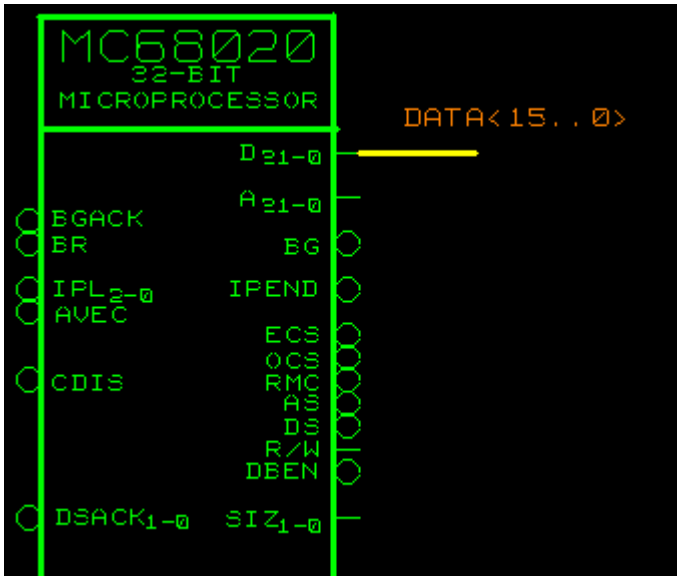
1. Choose *Wire – Draw*.
2. Draw a wire on pin D 31-0 as shown in the following figure.



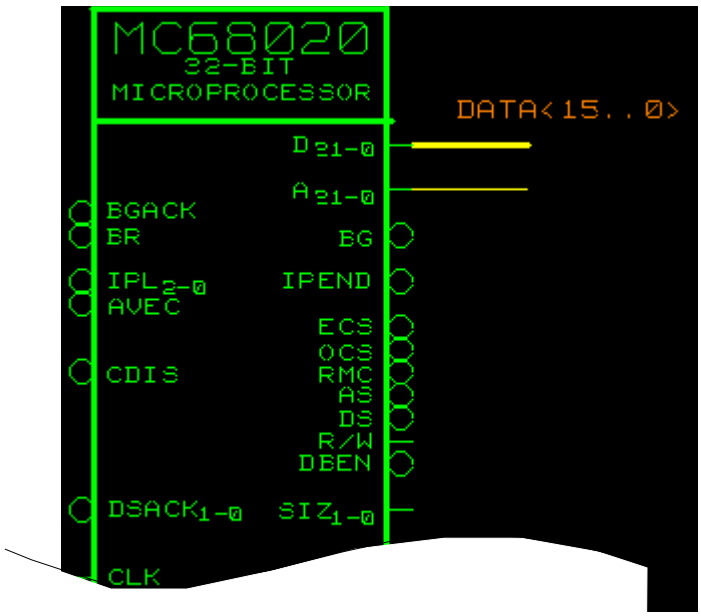
3. Choose *Wire – Signal Name*.

   The Signal Name dialog box appears.
4. Enter `DATA<15..0>` as the signal name.
5. Click the wire to name it.

Design Entry HDL attaches the name to the wire and thickens the wire to convert it to a 16-bit bus as shown in the following figure.



6. Next, add a 32-bit bus on pin A31-0.
7. Choose *Wire – Draw*.
8. Draw a wire on pin A 31-0 as shown in the following figure.



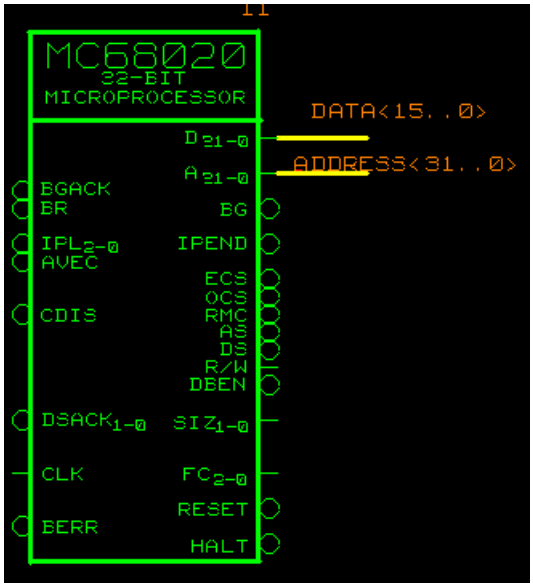
9. Choose *Wire – Signal Name*.

   The Signal Name dialog box appears.

10. Enter ADDRESS<31..0> as the signal name.

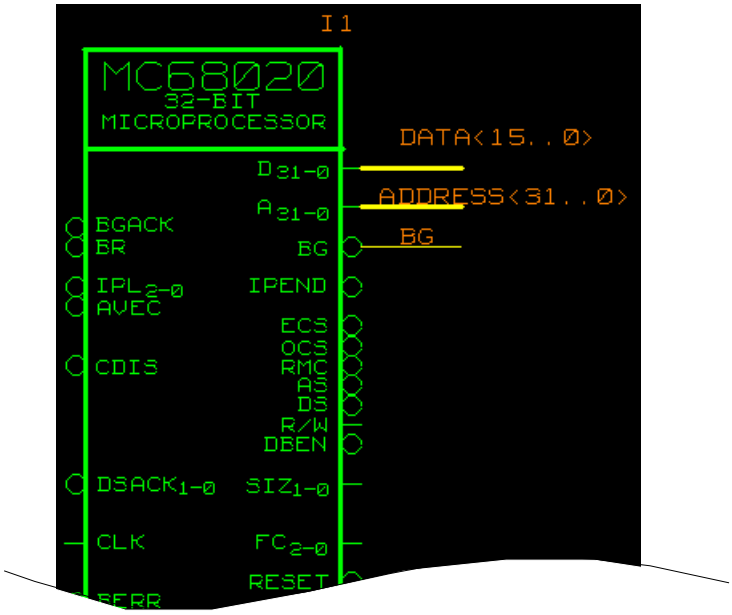
11. Click the wire to name it.

Design Entry HDL attaches the name to the wire and thickens the wire to convert it to a 32-bit bus as shown in the following figure.

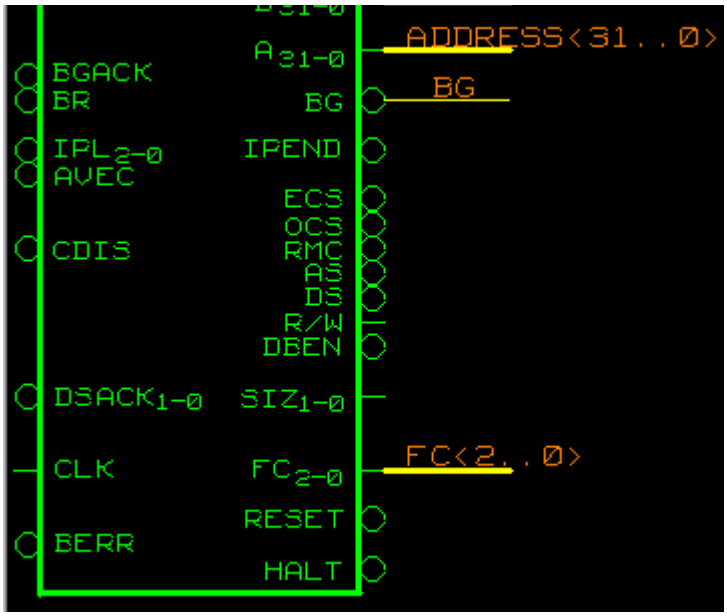


12. Add a wire to pin BG.

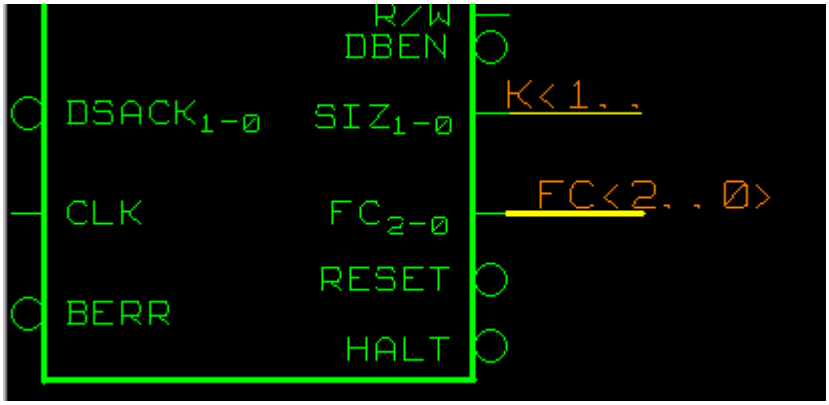
13. Specify BG as the name of the wire.



14. Add a 3-bit bus to pin *FC 2-0* as shown in the following figure.



15. Add a wire to *SIZ1-0* and name it *K<1..* as shown in the following figure.



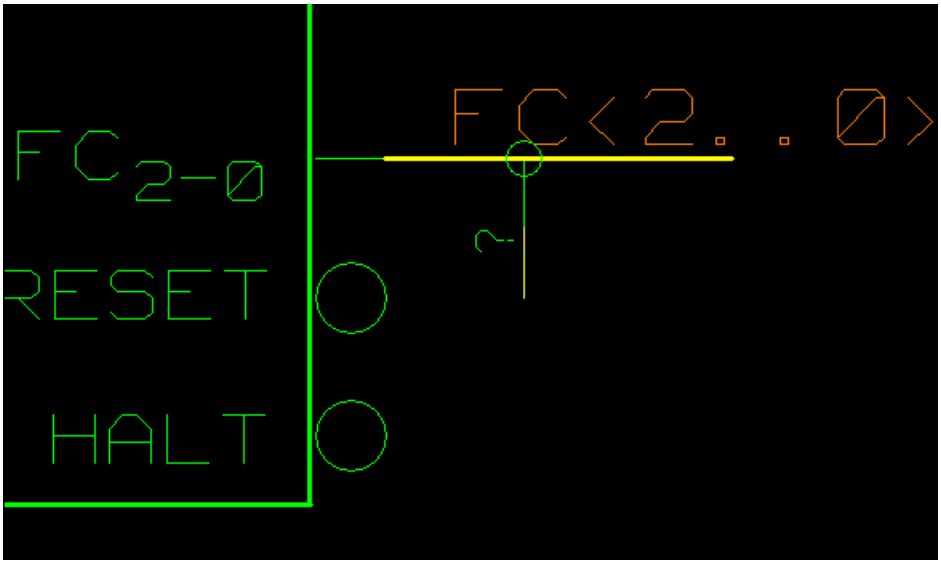
Tapping a Bus

While designing a circuit, you may use a particular bit from a bus as an input to a component in the circuit. To extract a particular bit from a bus, you tap a bus. In this section, you will tap the 3-bit bus, *FC<2..0>*, to extract the value stored in bit 1.

1. Zoom into *FC<2..0>*.

   Design Entry HDL zooms into the bus as shown in the following figure.

2. Choose *Wire – Bus Tap* to tap the bus.
3. Click *FC<2..0>* to place the bus tap symbol.
4. Extend the wire downwards, and double-click.
5. Right-click and choose *End Tap*.



   A question mark appears on the bus tap symbol. Replace this symbol with the bit number that is to be extracted.

6. Choose *Text – Change*.

7. Click the question mark.

   Design Entry HDL places a cursor on the question mark.

8. To indicate that you want to extract bit 1 in the schematic design, delete the question mark and enter 1.
9. Press `Enter`.

   Design Entry HDL marks 1 as the BN property (Bit Number) value.

   Note: If a tapped signal is not named, Design Entry HDL names the signal automatically.

Adding Physical Information

One of the factors that influence the PCB design is the behavior of components used in a circuit. A design is also influenced by factors such as temperature and component tolerance.

While creating a schematic design, you can specify the physical information of a component. The physical information is added on a component using the Physical Part Filter in Component Browser. The Physical Part Filter displays the Part Table File (`.ptf`) associated with a component or a library.

The Part Table File associates a logical part with physical parts having varying physical properties. Each row in the Part Table file (and in the Physical Part Filter) corresponds to a physical part.

Note: You can create a part table file using Part Developer.

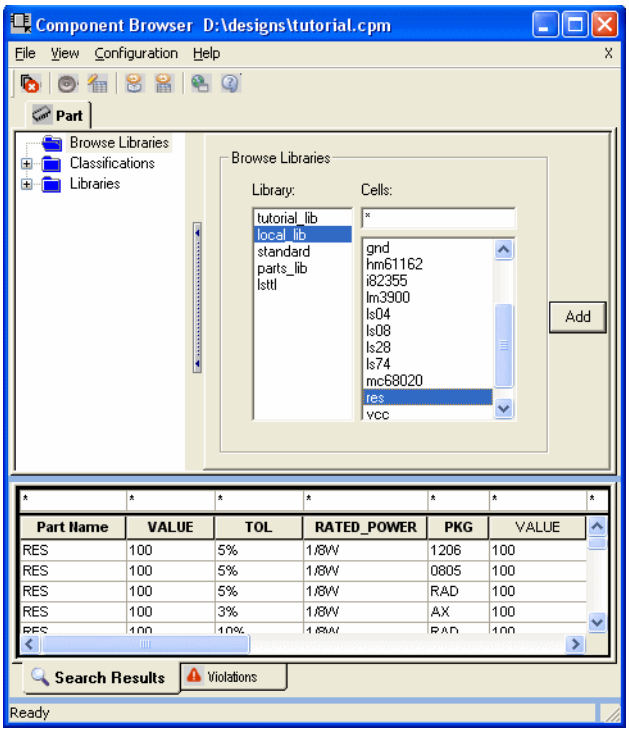
In this section, you will add a resistor and its physical information to the schematic design.

1. Choose *Component – Add*.

   Component Browser appears.

2. Select `local_lib` as the library.

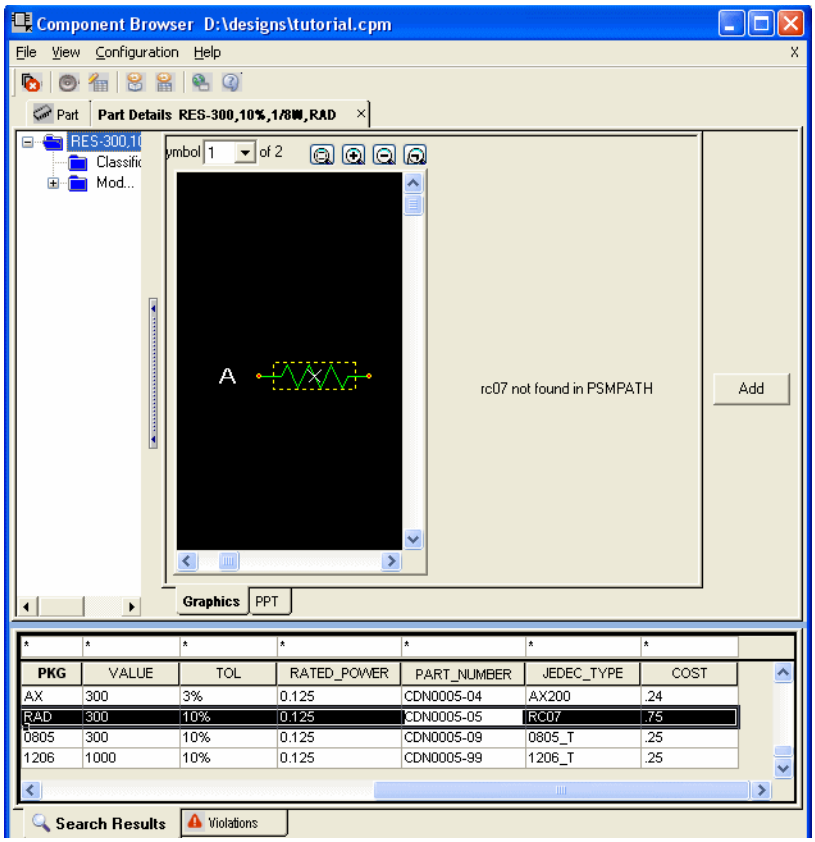
3. Select RES from the list and observe the *Physical Part Filter*.



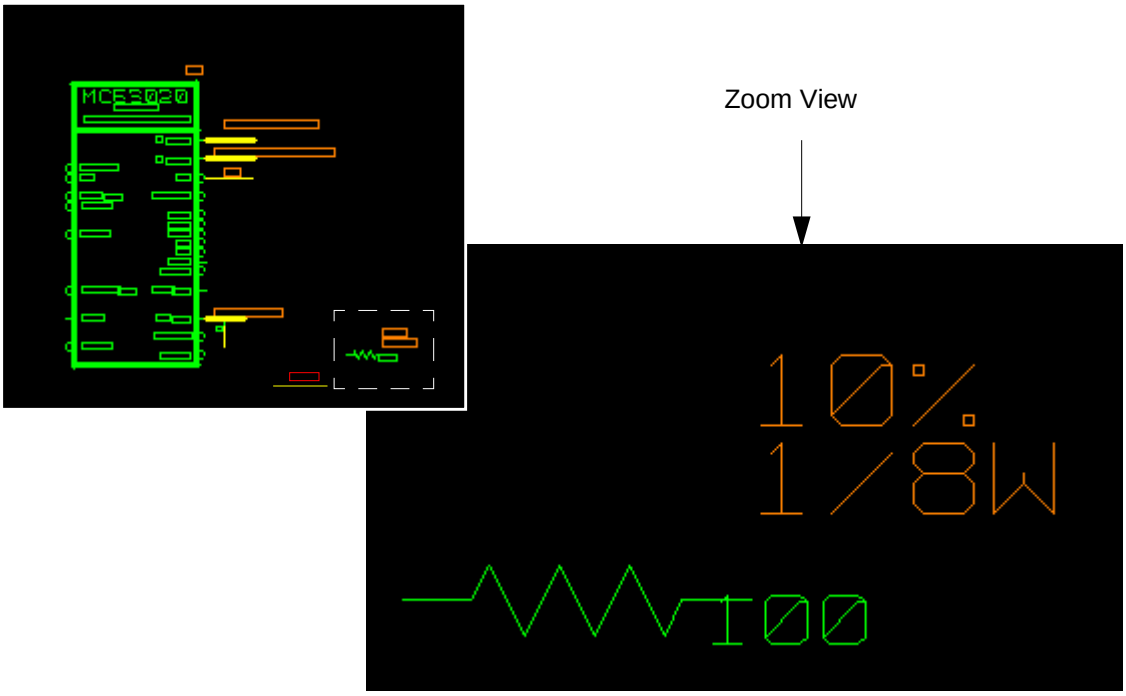
   While creating the schematic design, for optimum performance, the resistor value should be 100 ohms and the tolerance limit should be 10%.

4. Specify this information in the design using the *Physical Part Filter*.

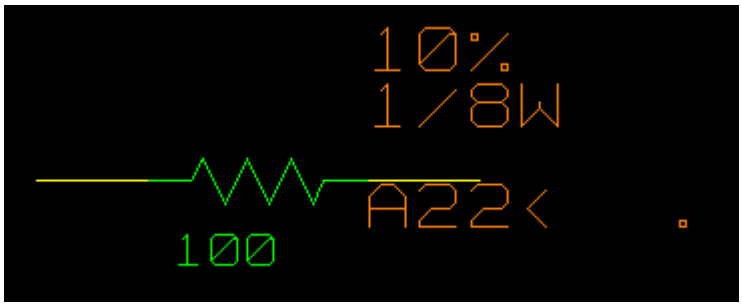
5. Select the row as shown in the *Physical Part Filter*.



6. Click the design window to place the part with the physical properties as shown in the following figure.



7. Add wires to RES as shown in the following figure.



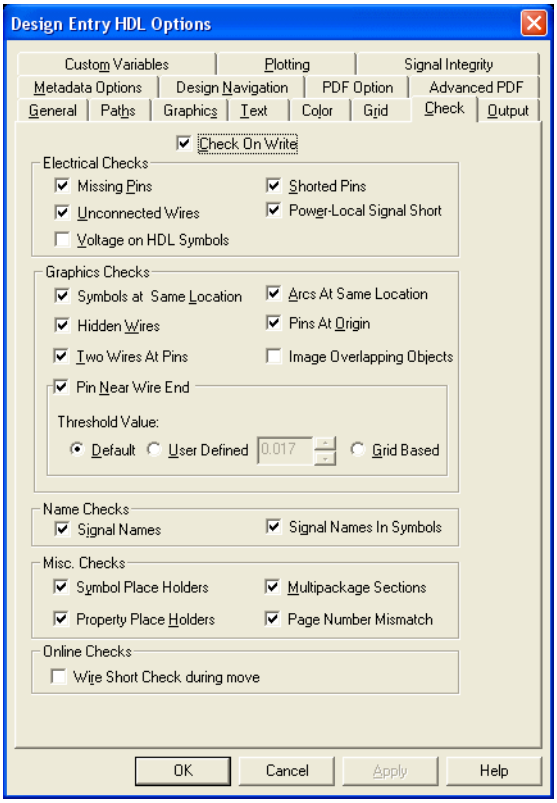
8. Specify A22 as the wire name.

Saving and Viewing Errors

Design Entry HDL runs various checks, such as electrical checks, graphic checks, and name checks, before saving the schematic design. You can change the default settings and specify the checks that should be performed by Design Entry HDL while saving any schematic.

1. Choose *Tools – Options – Check* to view the default settings or to change the settings.

   The Design Entry HDL Options dialog box appears.



   Note: Design Entry HDL performs various checks before saving a schematic because, by default, the *Check On Write* check box is selected. If you deselect this check box, Design Entry HDL will not perform any kind of checks while saving the schematics.

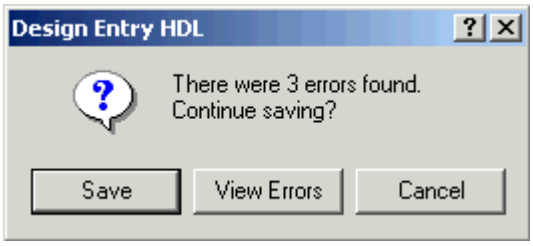
   For this tutorial, do not change the default settings.

2. Click *OK* to close the Design Entry Options dialog box.

   In addition to the checks available at *Tools – Options – Check*, Design Entry HDL also runs another set of checks for connectivity errors.

3. To save the schematics, choose *File – Save*.

The Design Entry HDL dialog box appears.

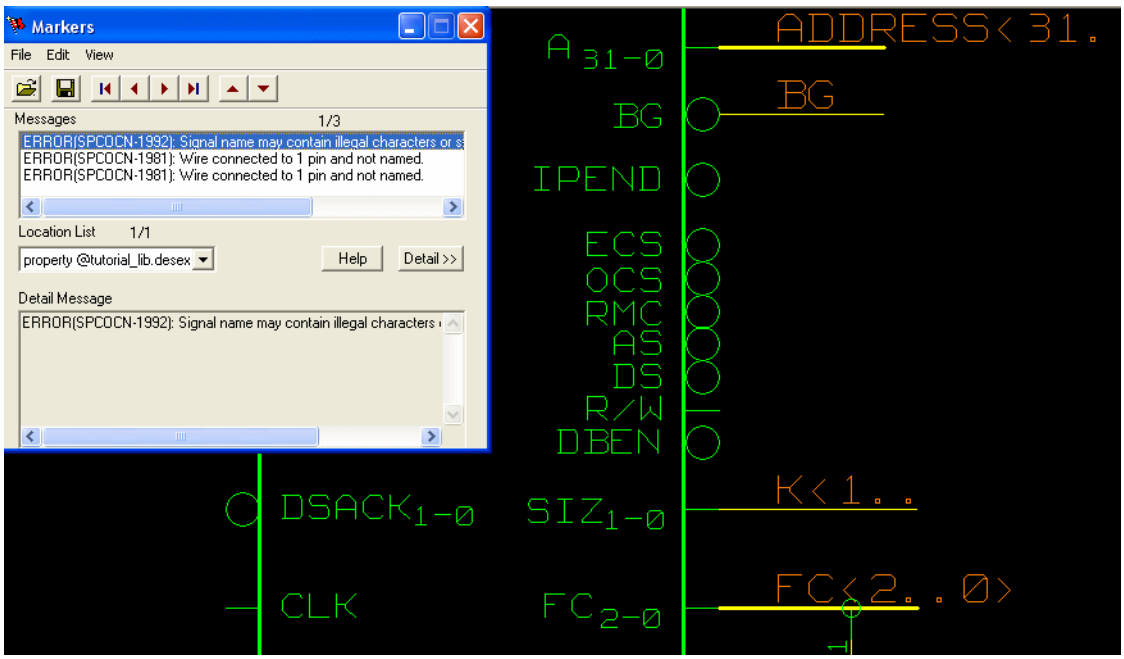


4. Click *View Errors*.

   The Markers dialog box appears displaying errors.

5. Select the first error.

   Design Entry HDL highlights the location of the error in the schematic.



   This error occurred because the syntax of the signal name is incorrect.

6. Right-click the signal name and select *Change*.

7. Change the name of the signal to `K<1..0>`.

8. Select the second error.

   Design Entry HDL highlights the location of the error in the schematic.

   This error is a result of an unnamed wire. Name the wire.

9. Choose *Wire – Signal Name*.

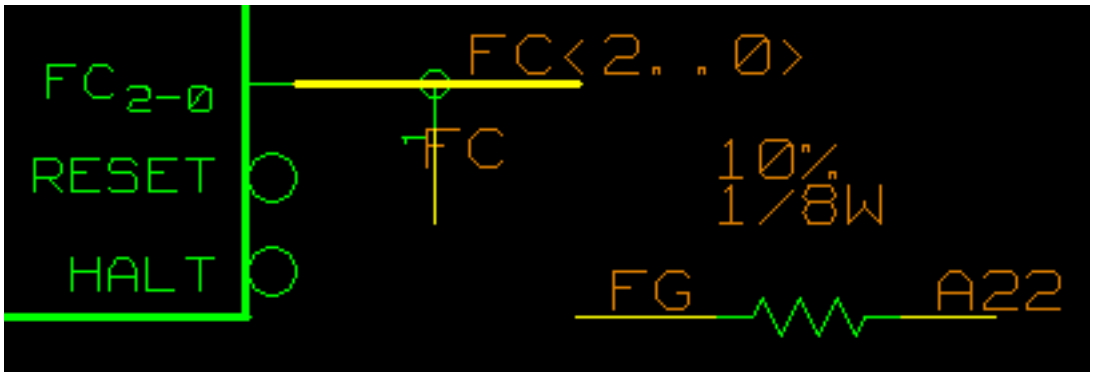
10. Select the third error.

    Design Entry HDL highlights the location of the error in the schematic.

    This error is also a result of an unnamed wire.

    Note: If the tap signal is connected to a component, Design Entry HDL automatically names it. In the preceding design example, the signal is not connected to any pin, so, we need to name it.

11. Choose *Wire – Signal Name* to name the wires as FG and FC as shown in the following figure.

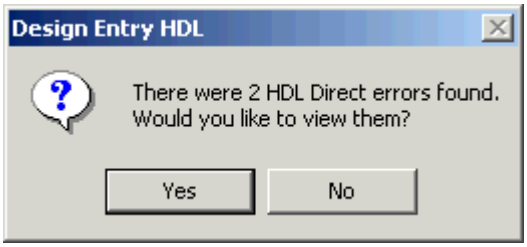


12. Click *Close*.

13. Close the Markers dialog box.

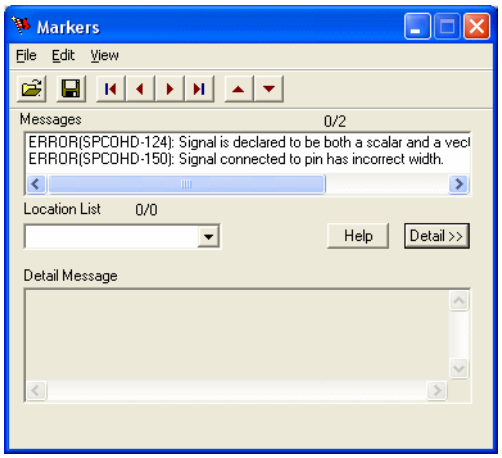
14. Choose *File – Save* again.

    Design Entry HDL runs a check for connectivity errors and reports them.



15. Click *Yes*.

The Markers dialog box appears displaying connectivity errors.



16. Select the first error.

Design Entry HDL highlights the location of the error in the schematic.

17. Choose *Text – Change* and change the wire name of *FC* to `FC1`.

18. Select the next error.

Design Entry HDL highlights the location of the error in the schematic.

This error occurred because a 16-bit bus is connected to a 32-bit pin.

19. Choose *Text – Change*.

20. Click `DATA<15..0>` and change it to `DATA<31..0>`.

21. Press `Enter`.

22. Choose *File – Close* to close the Markers window.

23. Choose *File – Save* to save the design.

Design Entry HDL saves the design you created without any errors.

4

Creating a Schematic: Advanced

This chapter contains the following information:

Using Groups

When you have multiple objects, such as parts and wires, that you want to move, copy, or perform other edit operations on, you can enclose them in a group and perform the operations on all of the objects together in the group. Groups are useful when you want to perform a single task on multiple objects.

Design Entry HDL provides the following three methods for creating groups:

- By Expression
- By Rectangle
- By Polygon

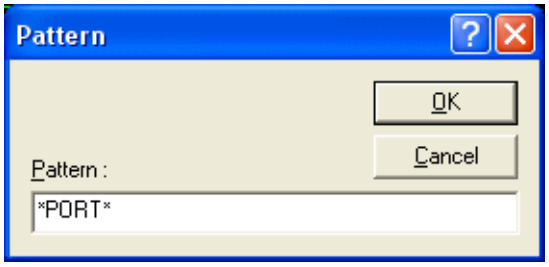
To create a group, you first need to open the schematic design. Run Project Manager, and load the tutorial project. When you open the project in Design Entry HDL, `DESEXAMPLE.SCH.1.1` is displayed.

Creating a Group By Expression

In this session, you will create a group of all objects in the schematic that have the text string `PORT` in their name.

1. Choose *Group – Create – By Expression*.

   The Pattern dialog box appears.



2. Type `*PORT*` in the *Pattern* field.
3. Click *OK*.

   Design Entry HDL highlights all objects in the schematic that include the test PORT in their names.

   By creating groups, you can delete, copy, or move multiple objects with PORT in their name in a single step.

4. To delete all objects in a group, choose *Group – Delete*.

   Design Entry HDL deletes all the objects in the group.

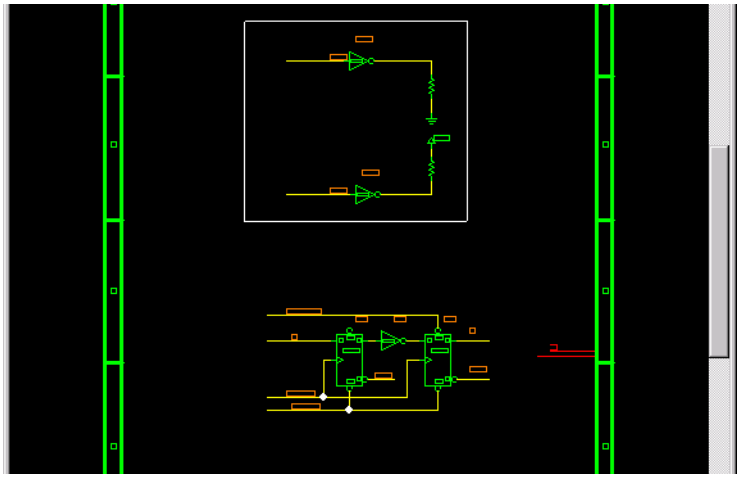
5. Choose *Edit – Undo* to reverse the deletion.

   Design Entry HDL places all the deleted objects back at their original positions in the schematic.

Creating a Group By Rectangle

The second method of creating a group is to select a part of the schematic design. The selection is done by drawing a rectangle. The part of the schematic design that is enclosed by the rectangle forms a group.

1. Choose *Group – Create – By Rectangle*.
2. Click, drag the mouse diagonally, and click again to create a rectangle that selects the objects to group as shown in the following figure.



3. To move the objects in the group to a different part in the schematic design, choose *Group – Move*.

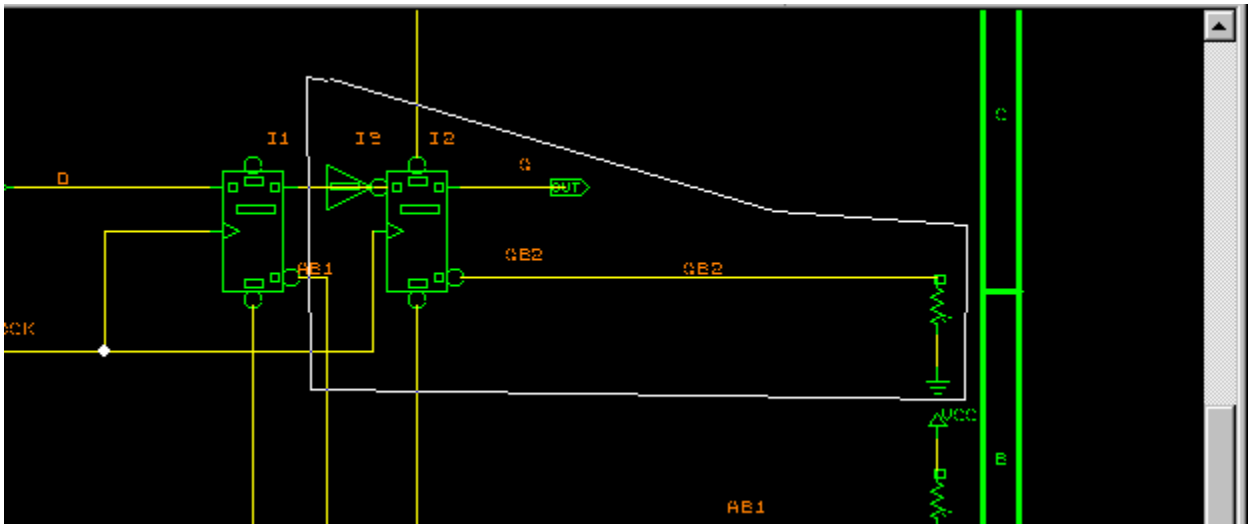
   The selected group attaches to the cursor.

4. Click a location in the schematic to place the group.
5. Right-click and choose *Done*.

Creating a Group by Using a Polygon

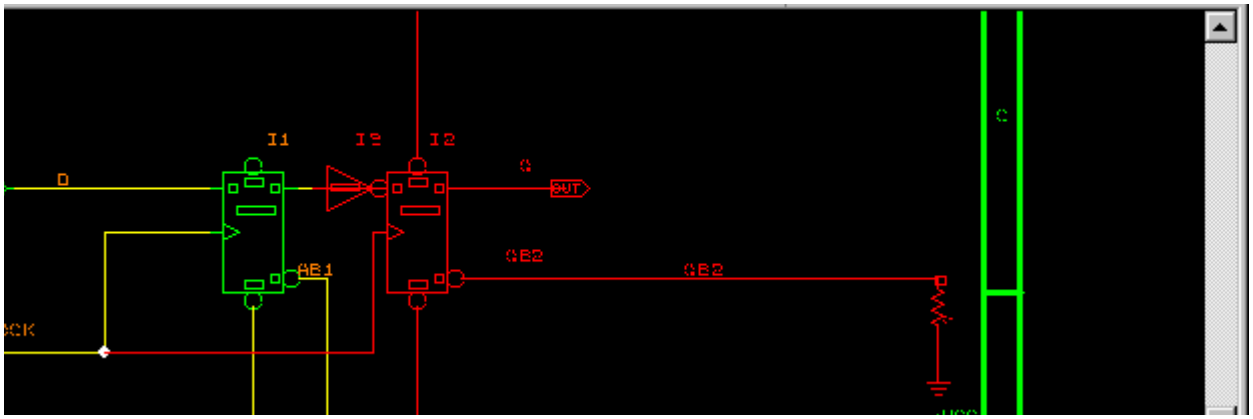
If a part of the schematic design cannot be enclosed within a rectangle, you can create a group by drawing a polygon that encloses the required part of the schematic.

1. To create a group by drawing a polygon, choose *Group – Create – By Polygon*.
2. Click, drag the mouse, and click again to draw one side of the polygon.
3. Complete the polygon as shown in the following figure.



4. Right-click and choose *Done*.

   The part of the schematic design within the polygon is highlighted in red.



You can now perform the required operations, such as copying, moving, and deleting, on the group.

Creating Hierarchical Designs

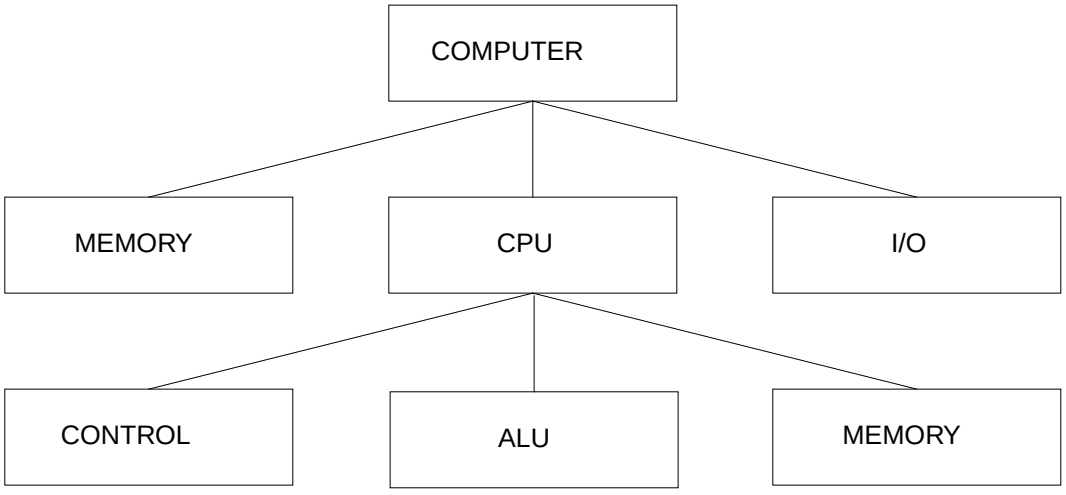
Use the hierarchical design technique to develop complex designs that comprise many modules. This method is useful for designs that reuse many of the same circuit functions, and for isolating portions of the design for teamwork assignments.

A hierarchical design results in print sets that are easy to read and the design produces modules that can be effectively debugged. Hierarchical designs, such as structured designs, reduce the amount of data entry and interconnections required by the design, thereby reducing the chances for errors. Creating a hierarchical design is a natural extension of the entire design process.

For example, if the design to be implemented is a computer, you begin the design by planning the parts of the computer. The computer can be divided into the CPU, MEMORY, and I/O modules. The CPU module can be further divided into the ALU, MEMORY, and CONTROL modules.

This represents three levels of hierarchy in the design. There are no limits to the number of levels you can include in a hierarchical design.

Figure 4-1 Levels of Hierarchy



To create a hierarchical design in Design Entry HDL, choose any of the following methods:

- Top down
- Bottom up

The Top-Down Method

In the top-down method, you visualize the design at a high level of abstraction. The schematic that represents this high-level of abstraction contains blocks that logically divide the design into subdesigns.

After the top-level design (also called the root design) is created with all the blocks, you create schematics that correspond to each block in the top-level schematic. These schematics can also have blocks that represent further logical divisions represented by lower-level schematics.

Use the top-down method when you clearly understand al aspects of the design. Before you create the design, you should know the interface signals with their directions (in, out, and inout).

Consider the computer example (see Levels of Hierarchy). In such a situation, to use a top-down approach, you start by creating the top-level schematic for COMPUTER. In this schematic, add blocks named MEMORY, CPU, and I/O. After naming these blocks, create schematics named MEMORY, CPU, and I/O.

In the CPU schematic, create three blocks: CONTROL, ALU, and MEMORY. After creating these blocks, create three corresponding schematics named CONTROL, ALU, and MEMORY.

Double-click a block in Design Entry HDL to descend into a lower level schematic. To ascend to a higher-level schematic, choose *File – Edit Hierarchy – Ascend*.

The Bottom-Up Method

In the bottom-up method, you create the schematics at the lowest level of the hierarchy. After the schematic is created, a symbol view is generated for this schematic by using `Genview` (Choose *Tools – Generate View* in Design Entry HDL). This symbol is instantiated (placed) on a schematic at a higher level in the hierarchy.

Continuing with the computer example (Levels of Hierarchy), here is how the bottom-up method would be applied. You would first create the schematics for the CONTROL, ALU, and MEMORY functions. After creating the schematics, use `GenView` to generate symbol views for each one of them.

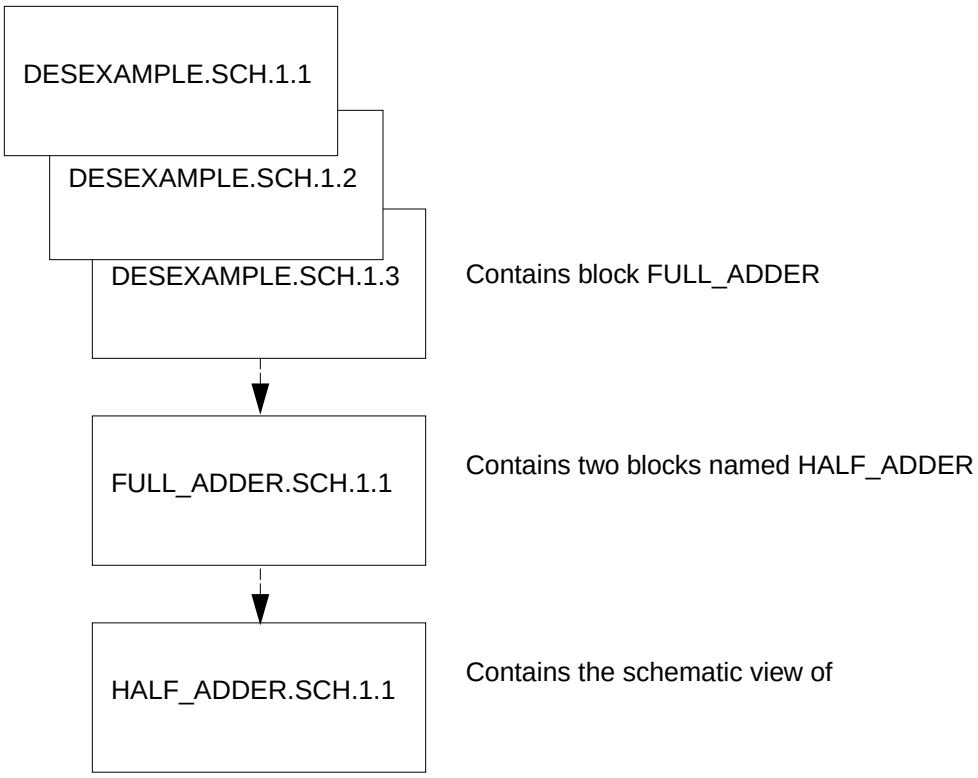
Next, you need to create the schematics for the subdesigns MEMORY, CPU, and I/O. In the schematic for CPU, instantiate the symbols for CONTROL, ALU, and MEMORY.

After the schematics at this level of hierarchy have been completed, generate symbols for each one of them. These three symbols can be instantiated to create the schematic for COMPUTER.

Creating a Hierarchical Design by using the Top-Down Method

In this section, the design discussed in the previous section (Levels of Hierarchy) will be created by using the top-down structure. The following figure displays the structure of the design that will be created.

Figure 4-2 Design Structure



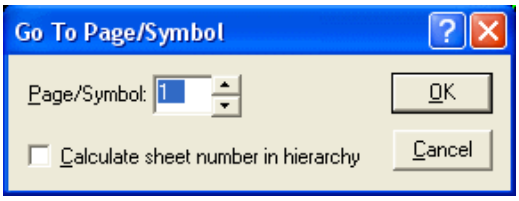
You need to perform the following tasks to implement the top-down approach for the preceding design:

1. Create a third page for the schematic view of DESEXAMPLE.
2. Add a block named FULL_ADDER to the third page,.
3. Create a schematic view for the block FULL_ADDER named FULL_ADDER.SCH.1.1.
4. In this schematic, add two blocks, both named HALF_ADDER.
5. After these blocks are connected, create the schematic view of HALF_ADDER in the schematic HALF_ADDER.SCH.1.1.

Now you are ready to start the procedure.

1. Open `DESEXAMPLE.SCH.1.1`.
2. Choose *File – Edit Page/Symbol – Go To*.

   The Go To Page/Symbol dialog box appears.

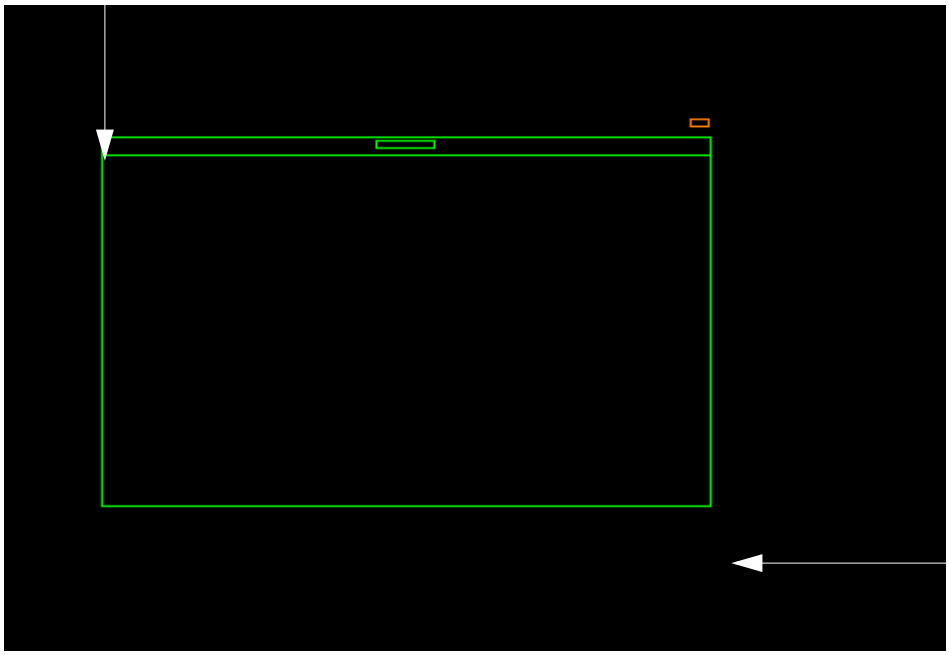


3. Enter 3 in the *Page/Symbol* field and click *OK*.

   Design Entry HDL prompts you for confirmation for creating a new page.
4. Click *Yes*.

   Design Entry HDL opens a blank schematic page named DESEXAMPLE.SCH.1.3.
5. To add a block FULL_ADDER to the page, choose *Block – Add*.
6. Click to begin drawing the rectangular block.

1. Click to start the rectangle.



2. Drag to draw the rectangle

3. Click to end drawing the rectangle and zoom into the selected area.

7. Drag the mouse diagonally to create a rectangle.
8. Click again to complete drawing the block.

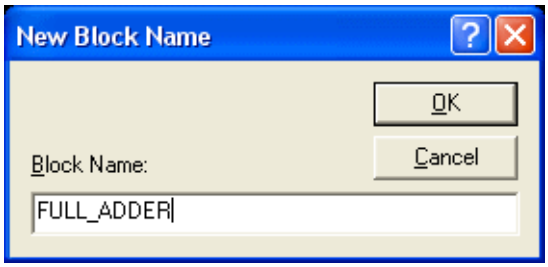
   Design Entry HDL displays the block, and by default, names the block as BLOCK1.
9. Right-click and choose *Done*.

Naming the Block

By default, the block is named BLOCK1.

1. Choose *Block – Rename* to change the name of the block.

   The New Block Name dialog box appears.
2. Type *FULL_ADDER* as the block name and click *OK*.



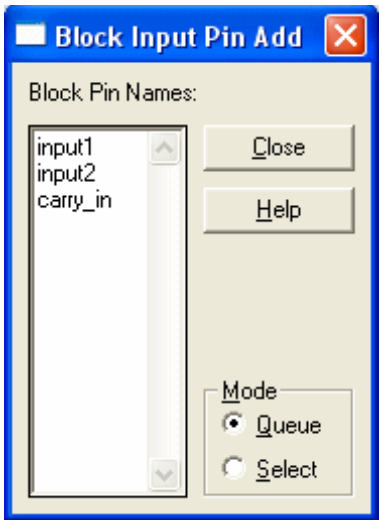
   Design Entry HDL attaches FULL_ADDER to the cursor.
3. Click the default block name, *BLOCK1*.

   Design Entry HDL replaces the block name *BLOCK1* with FULL_ADDER.
4. Choose *Block – Add Pin – Input Pin*.

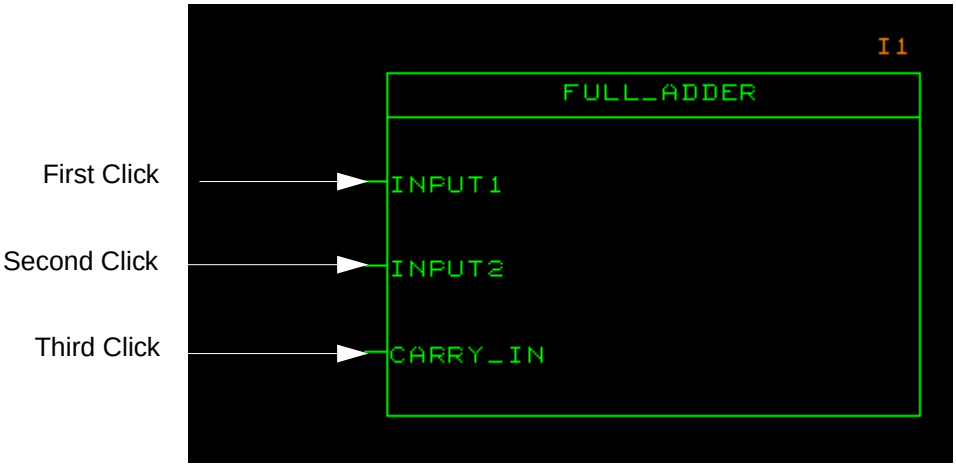
   The Block Input Pin Add dialog box appears.

5. Enter the following as input pins.

- input1
- input2
- carry_in



6. Place the input pins on the block as shown in the following figure.



7. Click *Close.*

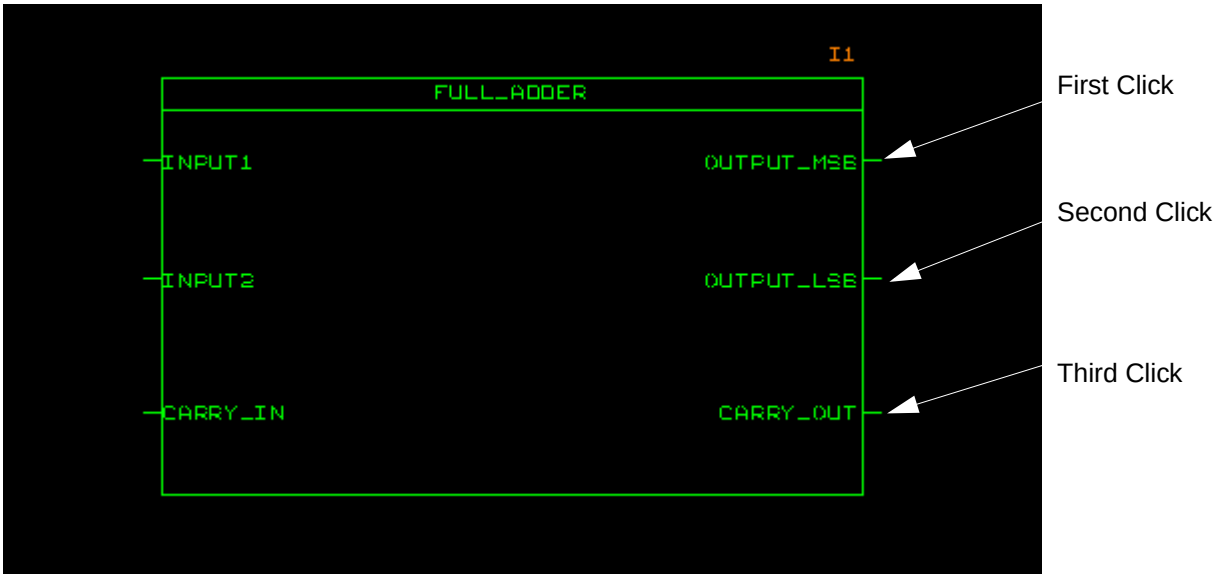
The *Block Input Pin Add* dialog box closes. Now, add output pins to the block.

8. Choose *Block – Add Pin – Output Pin*.

The Block Output Pin Add dialog box appears. In the dialog box, enter the following:

- output_msb
- output_lsb
- carry_out

9. Click the block to add pins as shown in the following figure.

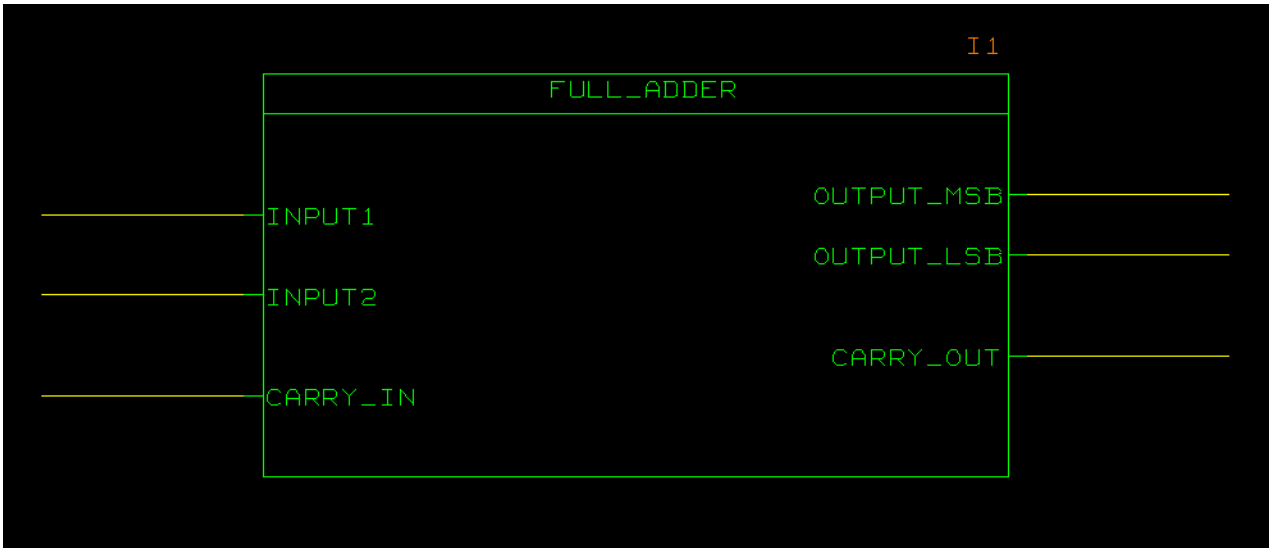


10. Click *Close.*

The Block Output Pin Add dialog box closes. Now, add wires to all the pins.

11. Choose *Wire – Draw*.

Add wires as shown in the following figure.



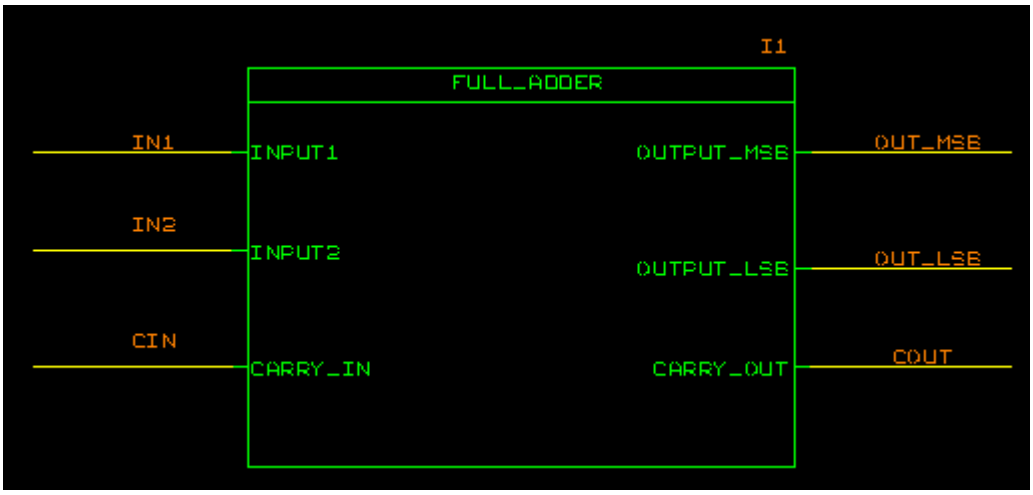
12. Choose *Wire – Signal Name*.

The Signal Name dialog box appears.

13. Specify the following signal names:

- IN1
- IN2
- CIN
- COUT
- OUT_LSB
- OUT_MSB

14. Click the wires to add the signals as shown in the following figure.



15. Click *Close*.

The *Signal Name* dialog box closes.

Adding Ports

Typically, input ports are placed on the left on the block, and output ports are placed on the right. The ports available in the `Standard` library (INPORT, OUTPORT) can be added using *Component Browser*.

1. Choose *Component – Add*.

The Component Browser dialog box appears.

2. Select `Standard` in the *Library* field.

3. Select `INPORT` and click *Add*.

4. Click at the end of the following wires:

- ❑ IN1
- ❑ IN2
- ❑ CIN

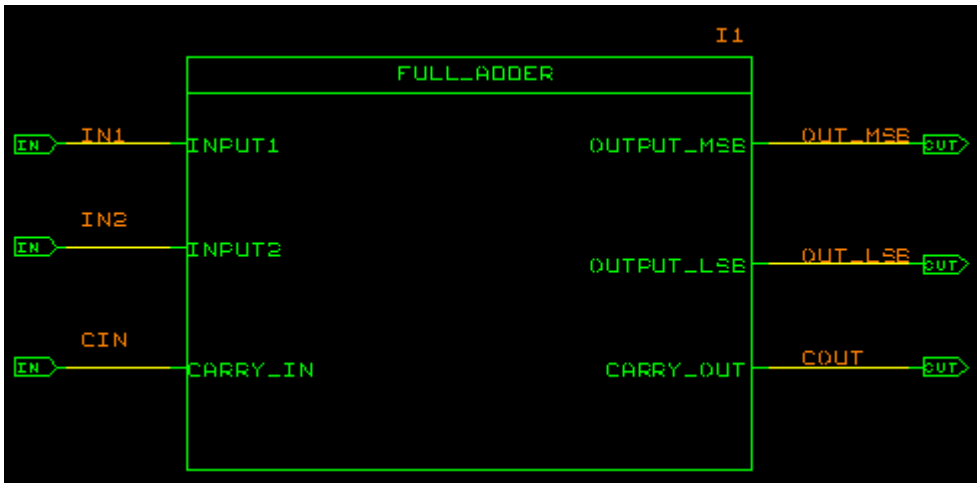
5. Select `OUTPORT` and click *Add*.

6. Click at the end of the following wires:

- ❑ COUT

- OUT_LSB
- OUT_MSB

The following figure displays the block FULL_ADDER with the ports.



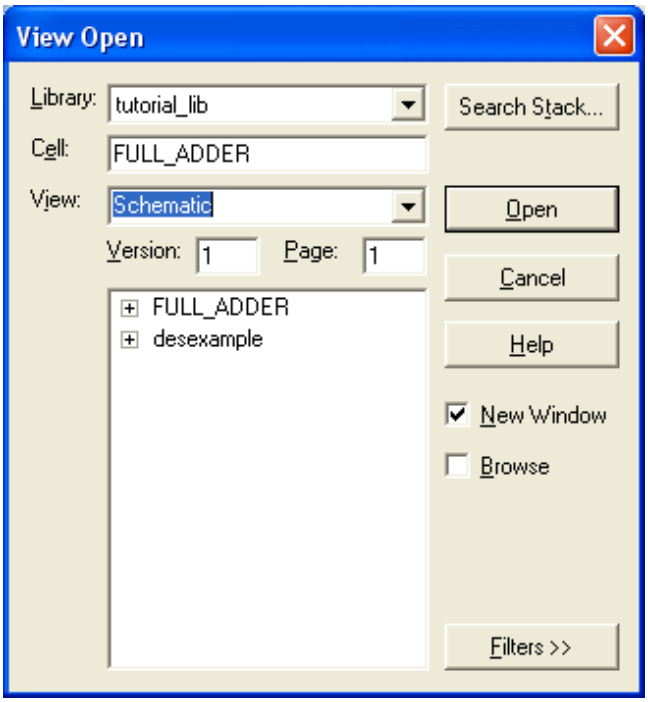
7. Choose *File – Close* to close Component Browser.
8. Choose *File – Save*.

Creating the Schematic View of FULL_ADDER

1. Choose *File – Open*.

   The *View Open* dialog box appears.
2. Select `tutorial_lib` as the *Library*.
3. Enter `FULL_ADDER` as the *Cell*.

4. Select `Schematic` as the *View*.



5. Click *Open*.

   Design Entry HDL opens a schematic page named `FULL_ADDER.SCH.1.1`.

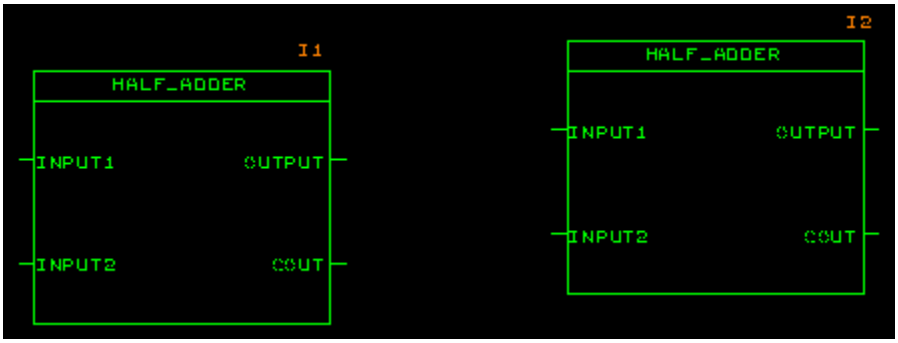
   In the schematic page, add a block.

6. Choose *Block – Add*.
7. Name it `HALF_ADDER` using *Block – Rename*.
8. Add the following input pins on the left of the block:
   - ❑ INPUT1
   - ❑ INPUT2
9. Add the following output pins on the right of the block:
   - ❑ OUTPUT
   - ❑ COUT

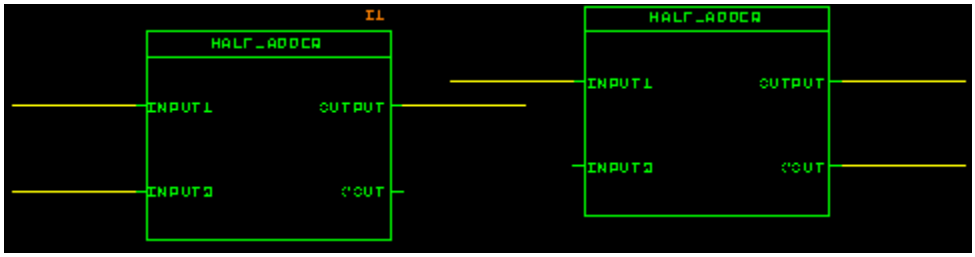
10. Choose *Edit – Copy* to copy.

11. Click the block *HALF_ADDER*.

12. Click to paste the copy as shown in the following figure.

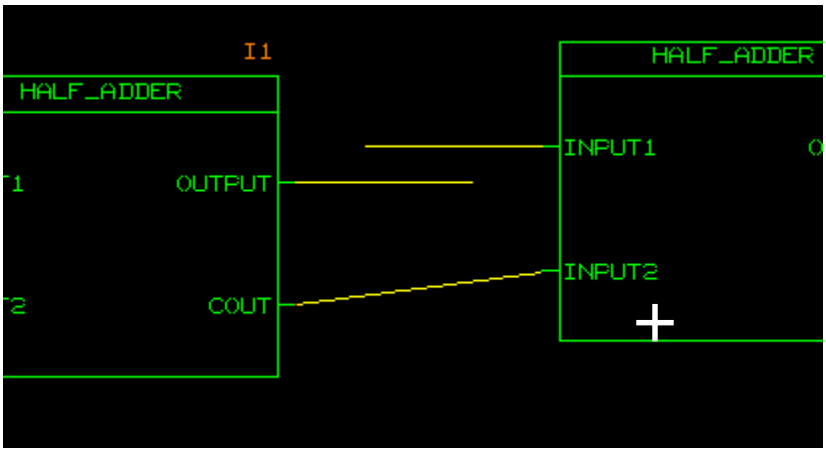


13. Choose *Wire – Draw* to draw wires as shown in the following figure.



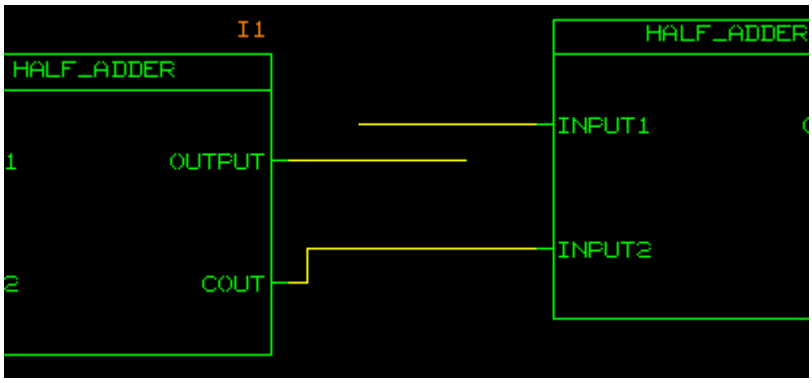
14. Choose *Wire – Route* to connect `COUT` and `INPUT2`.

15. Click at the tip of pin COUT and drag to the tip of pin INPUT2 as shown in the following figure.



16. Click again when the cursor touches the tip of INPUT2.

Design Entry HDL connects COUT and INPUT2 with a wire that bends at right angles as shown in the following figure.

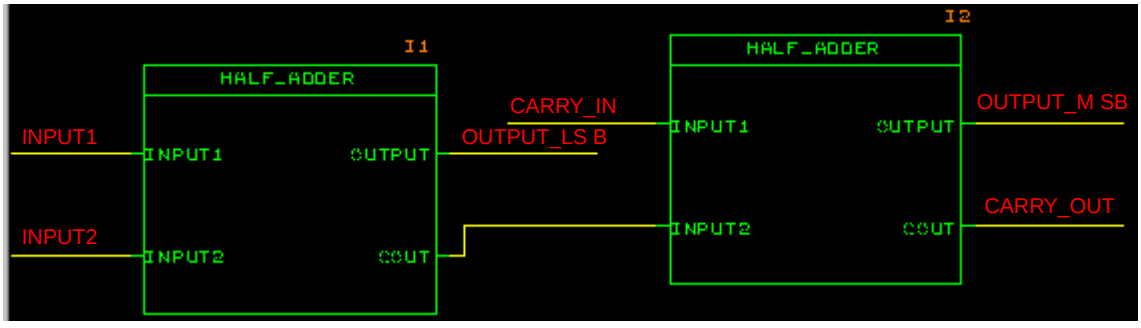


Add signal names. The signal names should be the same as that of the parent drawing.

17. Choose *Wire – Signal Name* to name wires with the following names:

- ❑ INPUT1
- ❑ INPUT2
- ❑ CARRY_IN
- ❑ CARRY_OUT
- ❑ OUTPUT_LSB
- ❑ OUTPUT_MSB

18. Assign names to the wires as shown in the following figure.



19. Add INPORTs to the following signals:

- ❑ INPUT1
- ❑ INPUT2

- CARRY_IN

20. Add OUTPORTs to the following wires:

- OUTPUT_LSB
- OUTPUT_MSB
- CARRY_OUT

Note: The signal names in the schematic diagram of a *HALF_ADDER* must be the same as the PIN names in the *FULL_ADDER* block.

21. Choose *File – Save* to save the design.

22. To view the FULL_ADDER block, choose *File – Edit Hierarchy – Ascend*.

Design Entry HDL displays `DESEXAMPLE.SCH.1.3` that contains the block `FULL_ADDER`.

23. Double-click the *FULL_ADDER* block.

Design Entry HDL descends into `FULL_ADDER.SCH.1.1`.

Creating a Schematic for HALF_ADDER

Finally, you create a schematic design for the HALF_ADDER block.

1. Choose *File – Open*.

   The View Open dialog box appears.

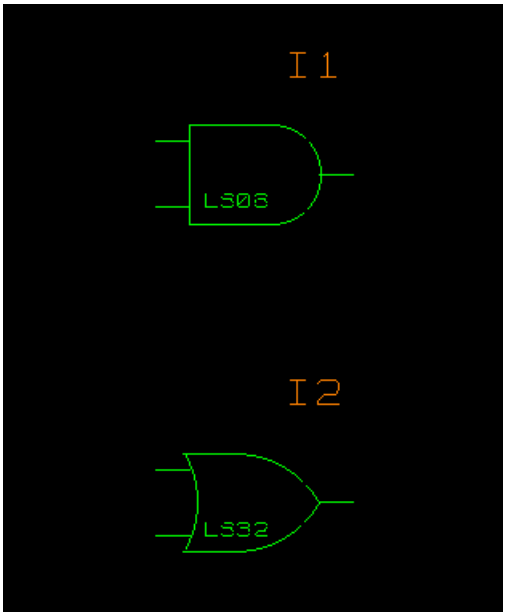
2. Select `tutorial_lib` as the *Library*.
3. Enter `HALF_ADDER` as the *Cell*.
4. Select `Schematic` as the *View*.
5. Click *Open*.

   Design Entry HDL opens a blank schematic page named HALF_ADDER.SCH.1.1 as shown in the following figure.

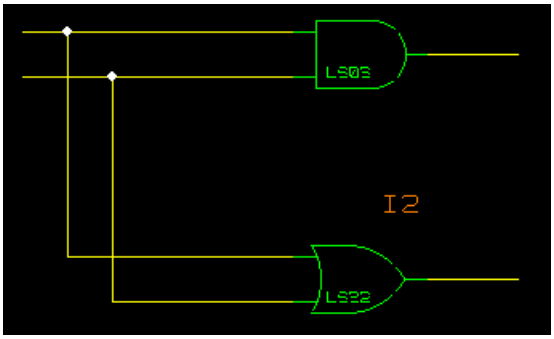
6. Choose *Component – Add*.

   Component Browser appears.

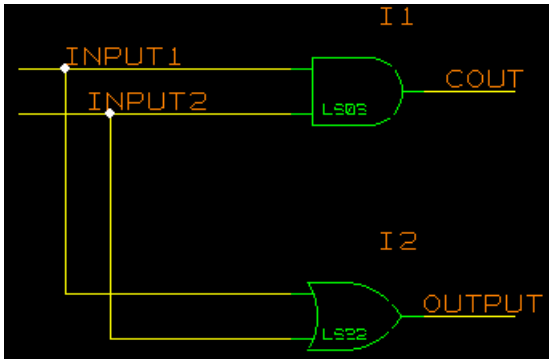
7. Select the `lsttl` library and the `LS08` cell.
8. Click *Add*.
9. Click the schematic to place *LS08*.
10. Select `LS32` from *lsttl* and place on schematic as shown in the following figure.



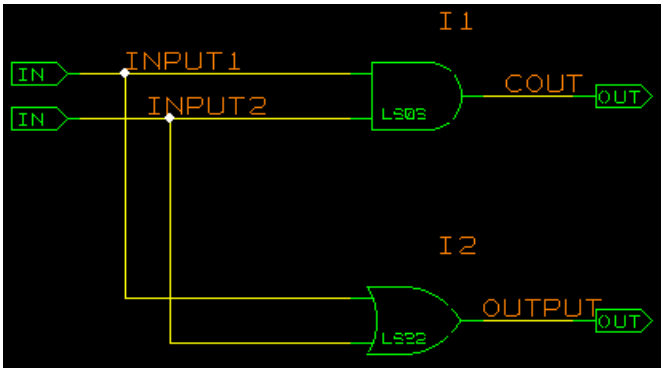
11. Choose *Wire – Draw* to connect the components as shown in the following figure.



12. Choose *Wire – Signal Name* to name the signals as shown in the following figure.



13. Add INPORTs and OUTPORTs from the `Standard` library as shown in the following figure.



14. Choose *File – Save* to save the design.

You have now created a multi-page hierarchical design using the top-down method.

15. To go through the entire design, starting from the top-level cell, choose *File – Open*.

The View Open dialog box appears.

16. Select `tutorial_lib` as the *library*.

17. Double-click DESEXAMPLE.

18. Double-click `sch_1`.

19. Select Page1 and click *Open*.

Design Entry HDL displays DESEXAMPLE.SCH.1.1.

20. Choose *File – Edit Page/Symbol – Next*.

Design Entry HDL displays `DESEXAMPLE.SCH.1.2`.

21. Choose *File – Edit Page/Symbol – Next*.

Design Entry HDL displays `DESEXAMPLE.SCH.1.3`.

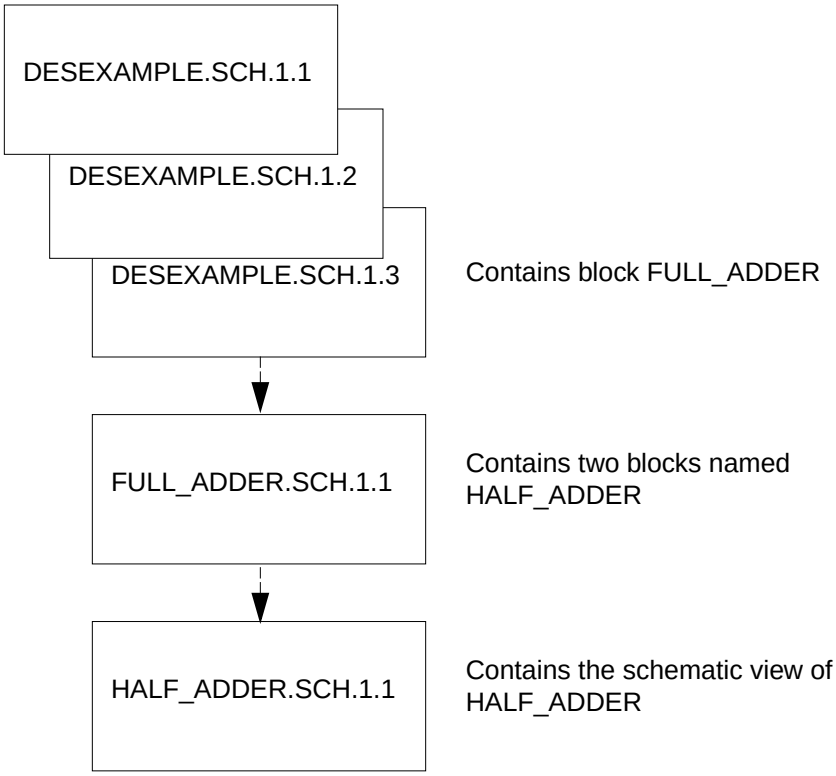
22. Double-click block FULL_ADDER.

Design Entry HDL displays `FULL_ADDER.SCH.1.1`.

23. Double-click a HALF_ADDER block.

Design Entry HDL opens `HALF_ADDER.SCH.1.1`.

The structure of the hierarchical design you have created is illustrated in the following figure.



Creating a Hierarchical Design Using the Bottom-Up Method

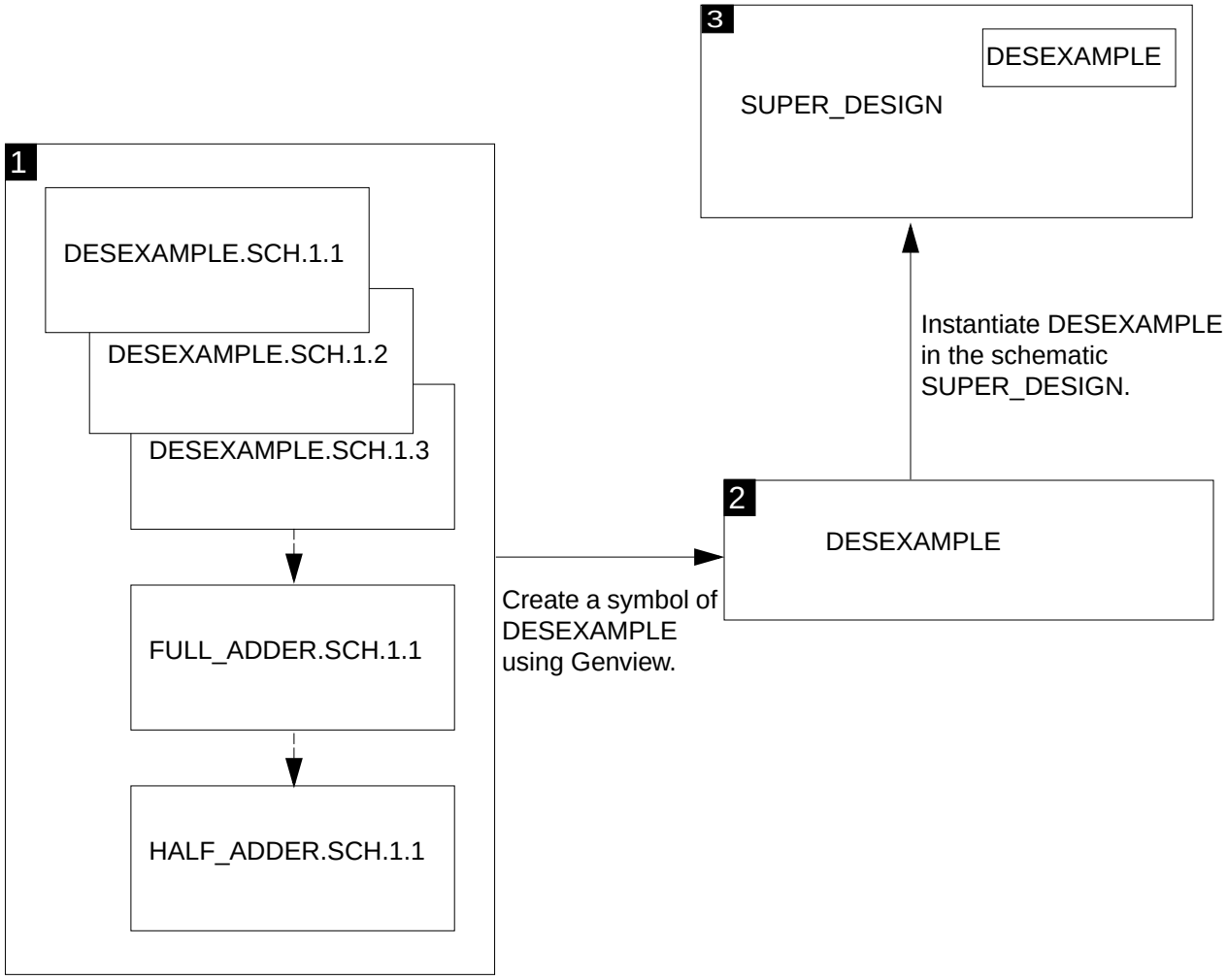
When you create a hierarchical design using the bottom-up method, you need to create a schematic page for the lower levels of the hierarchy and then add pages for the higher levels.

In the bottom-up method of creating a design, you perform the following steps:

- Create symbols for lower-level schematics.
- Create a schematic page for the higher design level and instantiate the symbols of the lower-level schematics in the schematic.
- Change the top-level design.

In this section, you use the design, DESEXAMPLE, as a lower-level design and add a schematic page called SUPER_DESIGN.SCH.1.1 at a higher hierarchical level. The following figure shows the planned design.

Figure 4-3 Bottom-Up Design

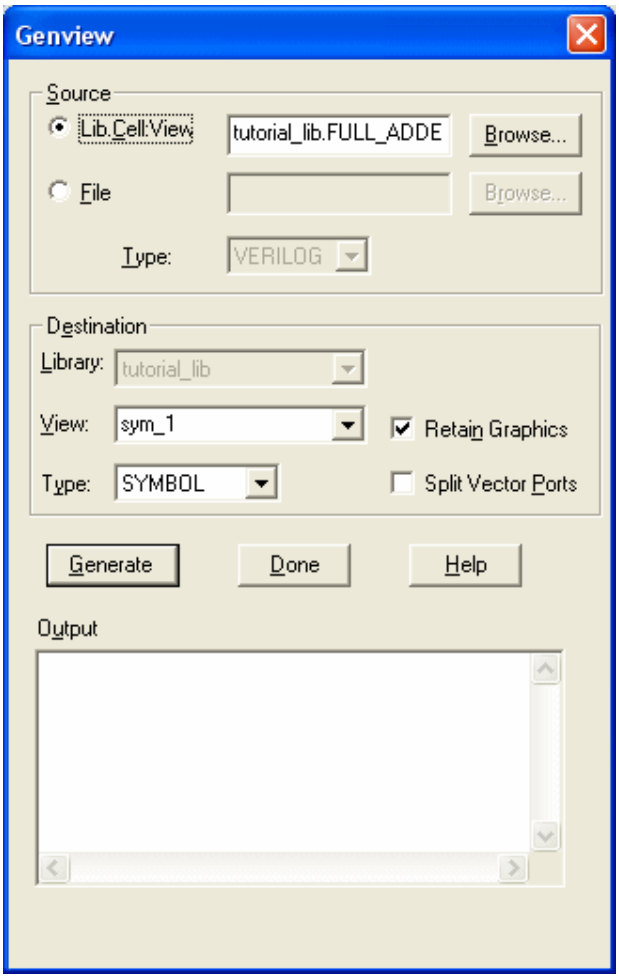


Creating a Symbol

1. Start Project Manager.
2. Load the tutorial project and open Design Entry HDL on the project.

   Design Entry HDL appears displaying DESEXAMPLE.SCH.1.1.
3. Choose *Tools – Generate View*.

The *Genview* dialog box appears.



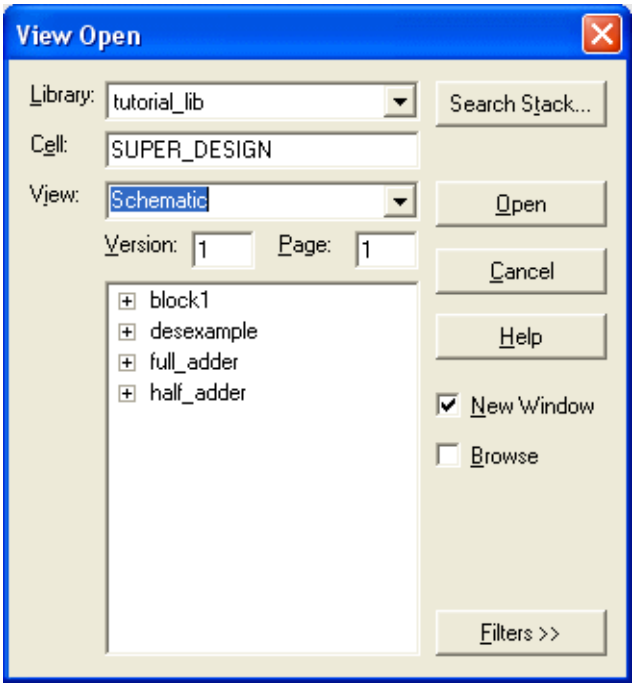
4. Click *Generate*.

   The Genview Status is displayed in the *Output* section of the Genview dialog box.

Creating a Schematic Page at a Higher Hierarchy Level

You will now create a new schematic page in which the symbol can be instantiated.

1. Choose *File – Open*.
2. Select `tutorial_lib` as the *library*.
3. Enter `SUPER_DESIGN` as the *Cell*.
4. Select `Schematic` as the *View*.



5. Click *Open*.

   Design Entry HDL creates a blank schematic page named SUPER_DESIGN.SCH.1.1.

6. Choose *Component – Add*.

   Component Browser appears.

7. Set *Library* as `tutorial_lib`.
8. Choose `Desexample` from the *Cells* list and click *Add*.

9. Click the Design Window to place the component.
10. Choose *File – Save* to save the schematic.
11. Choose *File – Exit*.

    Design Entry HDL exits.

Changing the Top-Level (Root) Design

In the design you have created, DESEXAMPLE is the top-level design. The top-level design is also known as the root design.

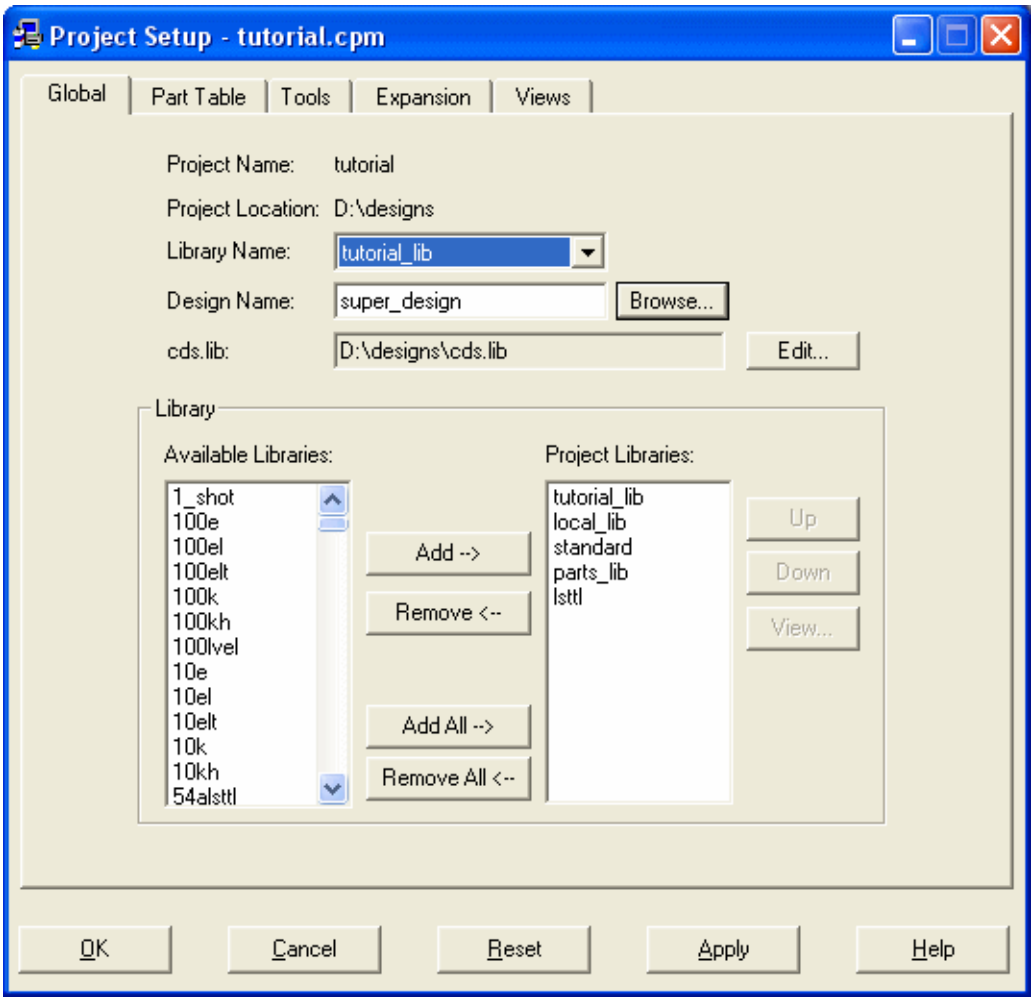
1. Click *Setup* in Project Manager.

   The Project Setup dialog box appears.

2. Click *Browse* next to the *Design Name* field.

   The Select Cell dialog box appears and it displays all the cells in `tutorial_lib` library.

3. Select `super_design` from the list.

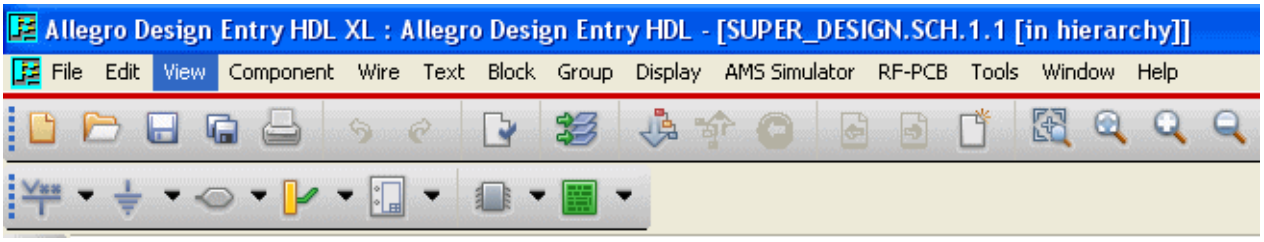


4. Click *OK*.

Project Manager changes the top-level design from `DESEXAMPLE` to `SUPER_DESIGN`.

5. Click *OK*.

To view the changes in the design structure, start Design Entry HDL by clicking *Design Entry* in Project Manager. Design Entry HDL opens SUPER_DESIGN_SCH.1.1.



Plotting a Schematic Design

At times you might require need to print your design for tasks, such as debugging and documentation. Design Entry HDL provides support for plotting your designs.

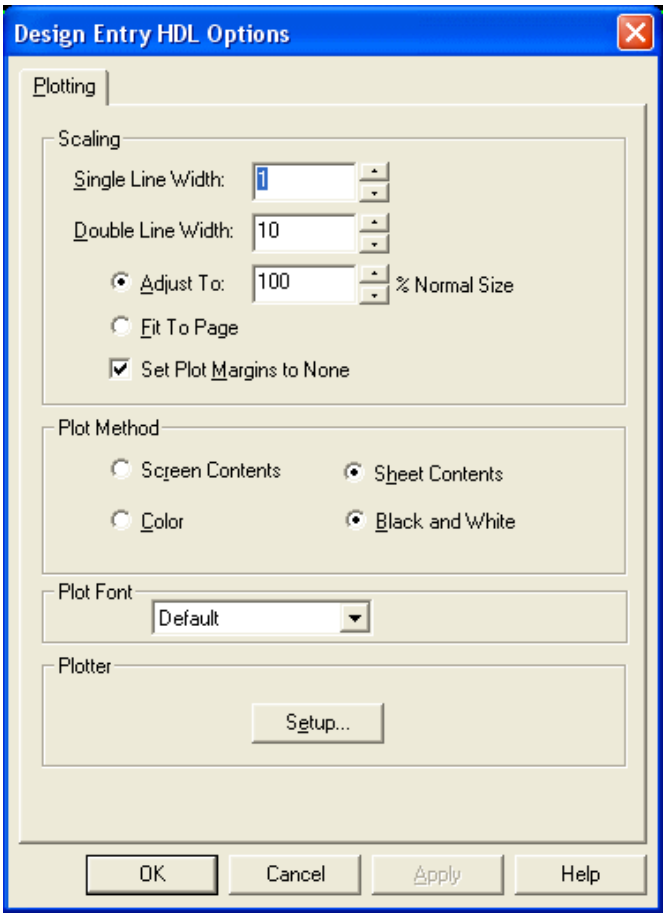
To plot a design, you need to perform the following steps:

- Setting up
- Previewing
- Plotting

Setting up the Plotting Options

1. To set up plotting, choose *File – Plot Setup*.

The Design Entry HDL Options dialog box appears with the *Plotting* tab.



You can also choose *Tools – Options* to display the Design Entry Options dialog box. By default, the *General* tab will be displayed. Then you select the *Plotting* tab.

Note: This dialog box appears only on Windows NT. On UNIX-based platforms, such as Solaris, HP, and IBM, the *Plotting* tab also has an option for *HPF Plotting*. This is because on UNIX-based platforms, Design Entry HDL provides two plotting modes, Windows Plotting and HPF Plotting.

To know more about the types of plotting see the *Plotting Your Design* chapter in *Allegro Design Entry HDL User Guide*.

2. In the *Scaling* section, accept the default values for *Single Line Width* and *Double Line Width*.
3. Select *Fit To Page* so that the complete schematic page is adjusted to fit into one page of the specified paper size.
4. Select a suitable *Plot Method*.

Select *Screen Contents* if you want to plot only that part of the design, which is visible on the screen. To plot the complete design, select *Sheet Contents*.

For the current design, select *Sheet Contents*.

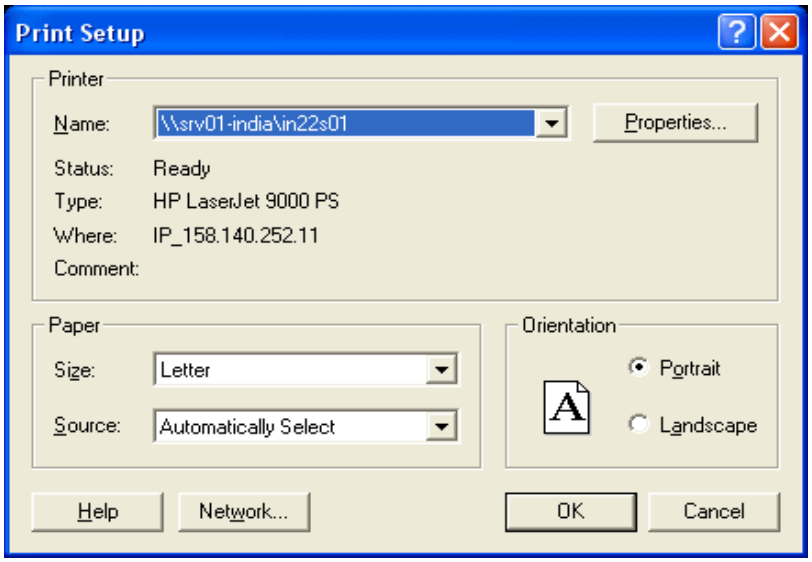
5. Select *Color* if you want to plot the drawing in color.

   Select *Black and White* to plot drawings in black and white. If you select *Color* on a black and white plotter, the printout has different scales of gray.

   For the current design, select *Black and White*.

6. Click *Setup*.

   The *Print Setup* dialog box appears.



7. Choose the `Plotter Name` from the list of plotters configured with the system.

   For the current design example, accept the default plotter.

8. Choose *Paper Size* and *Source*.

   In this example, we will accept the default values.

9. Specify the *Orientation* as `Landscape`.

10. Click *OK* to save the settings and to close the Print Setup dialog box.

11. Click *OK* to save the settings and to close the Design Entry Options dialog box.

Previewing the Plot

Before you take a printout of the design, it is a good practice to preview the design. If the preview is not according to your requirements, you can modify the setup.

1. To preview the design, choose *File – Plot Preview*.

   The complete schematic page is adjusted to fit into one sheet of the paper.

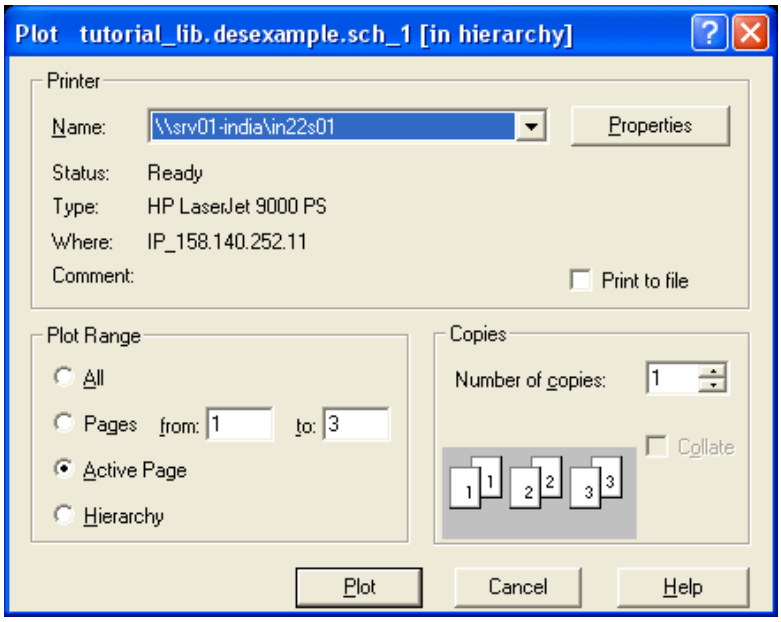
2. Click *Close* to close the preview window.

   Note: You can plot the design from the preview window. To plot the design, click *Print*.

Plotting the Design

1. To plot the design, choose *File – Plot*.

   The Plot dialog box appears.



   Note: The above dialog box appears on Windows NT. On UNIX based platforms, the dialog box shown above will appear only when you are in Windows Plotting. In HPF Plotting, if you choose *File – Plot,* the HPF Plot dialog box appears.

2. Click *Plot* to plot the design.

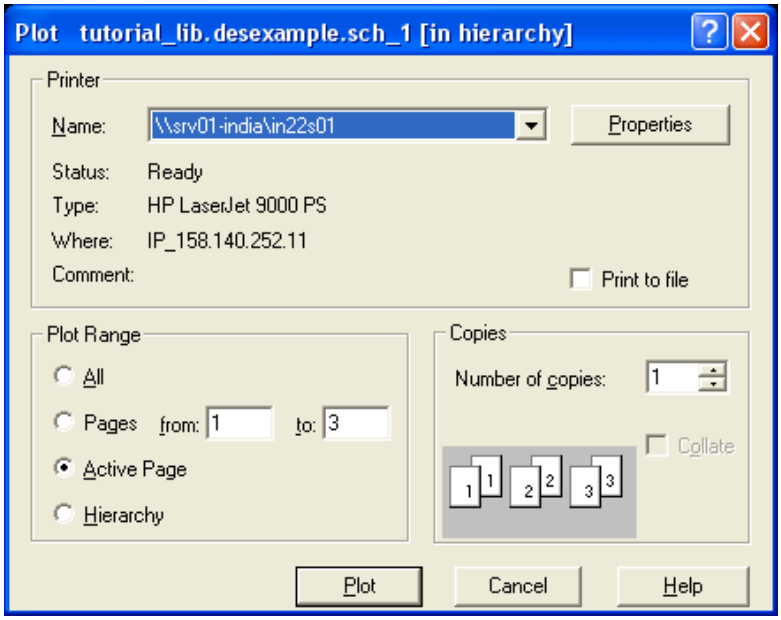
Hierarchical Plotting

An important feature supported by Design Entry HDL is hierarchical plotting. This feature is available in both Windows Plotting and HPF Plotting. For more information on Windows Plotting and HPF Plotting, see the *Plotting Your Design* chapter in *Allegro Design Entry HDL User Guide*.

Using hierarchical plotting, you can customize the way in which you plot various hierarchies in your design. To know more about how you can re-organize modules in your design, see *Module Ordering* in *the Working with Designs* chapter of the *Allegro Design Entry HDL User Guide.*

1. To plot the hierarchies in your design, choose *File – Plot*.

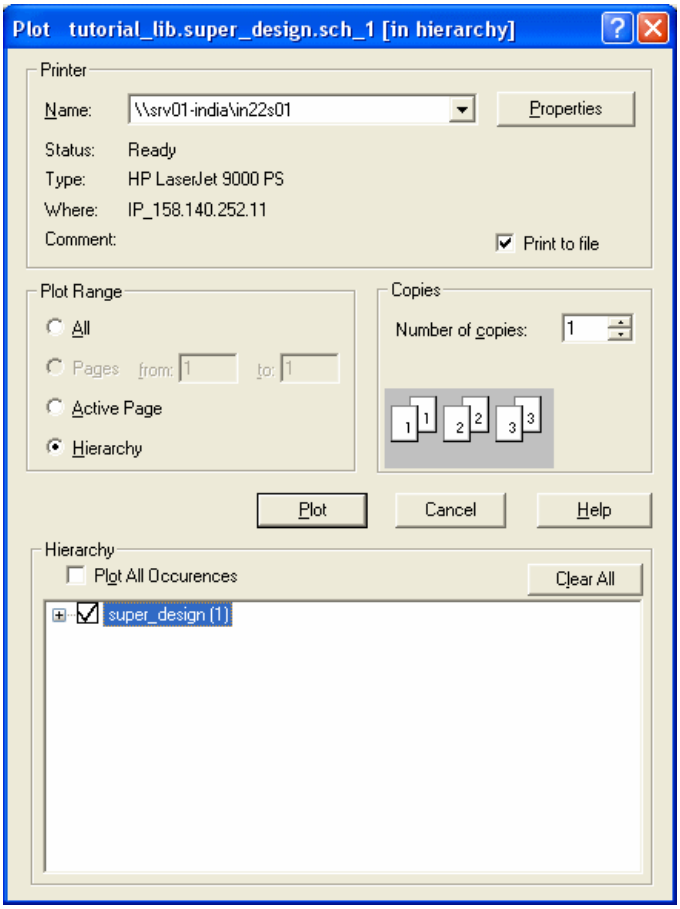
   The *Plot* dialog box appears.



   Note: The *Print to file* check box in the *Plot* dialog box appears only on Windows computers.

2. In the *Plot Range* section select `Hierarchy`.

The Hierarchy section appears with a tick mark against the design name.

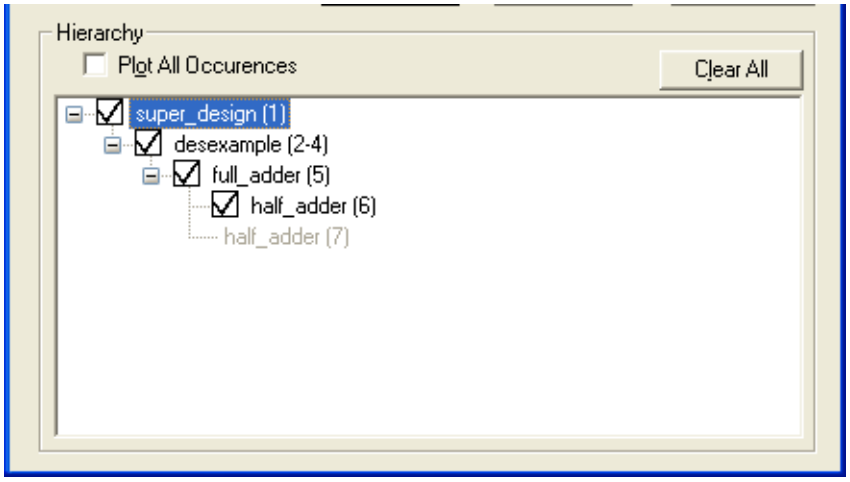


The tick mark indicates that all subdesigns under the design name `super_design` will be plotted.

Note: The hierarchy tree visible in the hierarchy section of the dialog box is same as the module ordering tree.

3. To expand the design, click the + sign.

A list of subdesigns under the design appear. Similarly, you can descend further down the hierarchy.



There are two occurrences of the block `half_adder` in the above figure. The second occurrence of the block `half_adder` is grayed out. This is because, in the Hierarchy or Expanded mode, only one occurrence of a block is plotted by default.

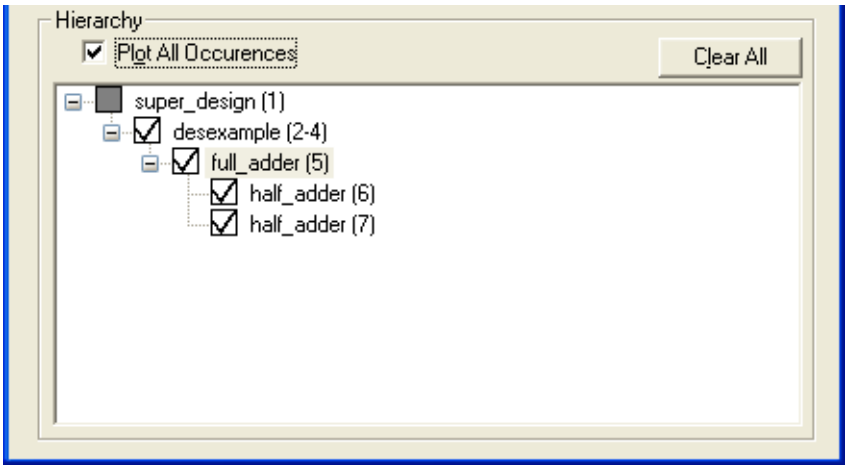
Note: In the Occurrence Edit mode, all occurrences of blocks are plotted by default.

4. Select the *Plot All Occurrences* check box to plot both the occurrences of the block `half_adder` in the design.

   Note: The *Plot All Occurrences* check box is displayed only if you are in the Hierarchy or Expanded mode.

   Using the hierarchical plotting, you can decide the subdesign that you want to plot. The tick mark indicates the designs that the design will be plotted. If you do not want to plot a particular design, deselect the tick mark against the design.

For example, if you do not want to plot `super_design` but only the subdesigns under it, deselect the tick mark against `super_design` as shown below.



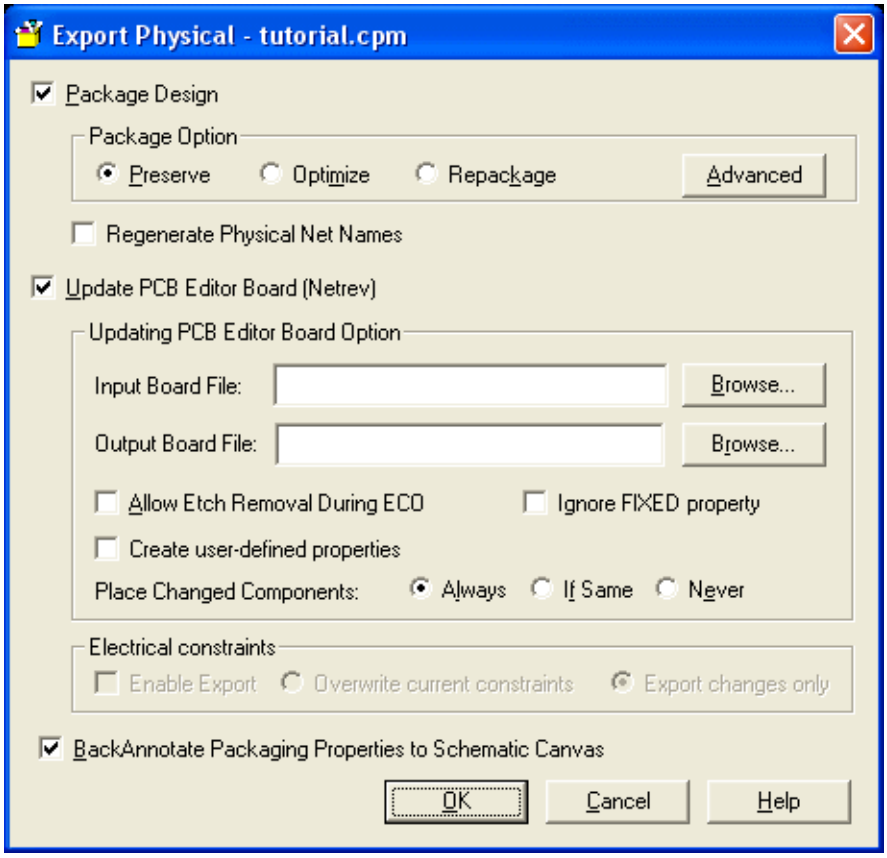
5. Click *Plot*.

Packaging Your Design

Packaging involves translating your logical design (schematic) captured into a physical design ready for placement and routing. The tool used for performing placing and routing is PCB Editor.

1. Choose *File – Export Physical*.

   The Export Physical dialog box appears as shown in the following figure.

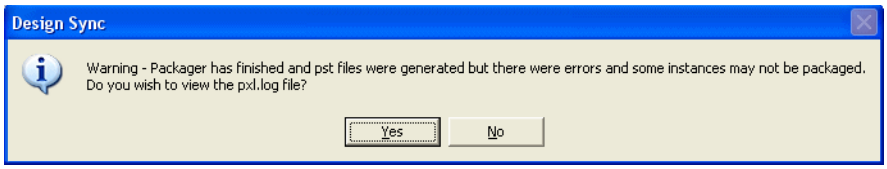


2. Select *Repackage*.
3. Deselect the *Update PCB Editor Board (Netrev)* check box.
4. Click *OK*.

   While packs

5. Click *Yes* when prompted to view the log file.

6. Click *Yes* when prompted to open the log file.



The log file is opened in a text editor. The log file lists the following two errors in assigning physical parts:

```
 ****************************************
 *  Starting to assign physical parts.  *
 ****************************************
#1  ERROR(1053): Cannot find a ppt part that matches the instance properties.
        Ppt Name: RES
       Schematic instance: @TUTORIAL_LIB.SUPER_DESIGN(SCH_1):PAGE1_I1@TUTORIA~
L_LIB.DESEXAMPLE(SCH_1):PAGE1_I15@LOCAL_LIB.RES(CHIPS)
        Property Name: VALUE
        Property Value: 100
        Property Name: TOL     (OPT=5%)
        Property Value:
        Property Name: RATED_POWER
        Property Value:
        Property Name: PKG
        Property Value: RAD
 #2  ERROR(1053): Cannot find a ppt part that matches the instance properties.
        Ppt Name: RES
       Schematic instance: @TUTORIAL_LIB.SUPER_DESIGN(SCH_1):PAGE1_I1@TUTORIA~
L_LIB.DESEXAMPLE(SCH_1):PAGE1_I16@LOCAL_LIB.RES(CHIPS)
        Property Name: VALUE
        Property Value: 100
        Property Name: TOL     (OPT=5%)
        Property Value:
        Property Name: RATED_POWER
        Property Value:
        Property Name: PKG
        Property Value: RAD
**********************************************
 *  End assigning physical parts.  (00:00:00)  *
 **********************************************

 ***************
```

```
 *  Packaging  *
 ***************

 ******************************
 *  End packaging  (00:00:00)  *
 ******************************

2 errors detected
No warnings detected
    Start time   10:06:07
    End time     10:06:35
    Elapsed time  0:00:28

 ********************************************
 *  ERROR Packager-XL exiting with status 1  *
 ********************************************
```

The errors in assigning physical parts occurred when Packager-XL matches the part table information for the component RES with the properties present on the component and is unable to match any row in the part table file with the properties on the component.

7. Close the text editor.
8. Click *Close* in the Progress window.

You will now use the *Global Find* utility in Design Entry HDL to locate the parts in the design named RES.

Using Global Find

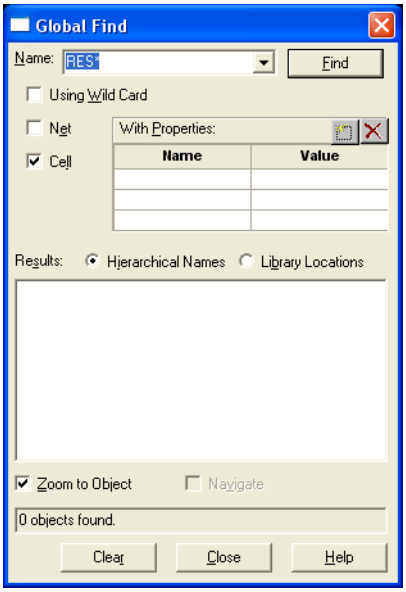
1. Choose *Tools – Global Find*.

   The Design Entry HDL message box appears.

2. Click *Yes*.

   Design Entry HDL expands the design and displays the Global Find dialog box.

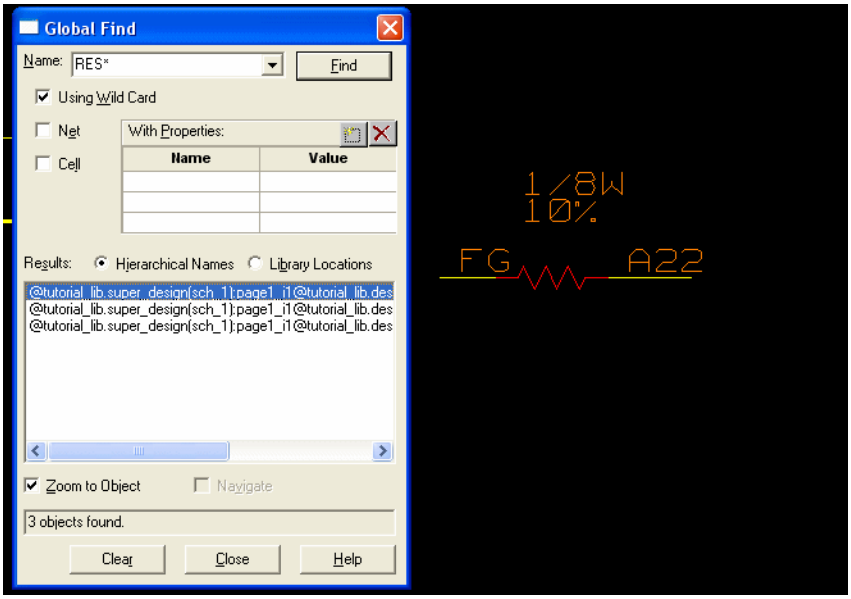
3. Type RES in the *Name* field.



Design Entry HDL locates three instances of RES in the design and displays the Hierarchical names in the Results field.

4. Click the first instance of RES in the *Results* field.

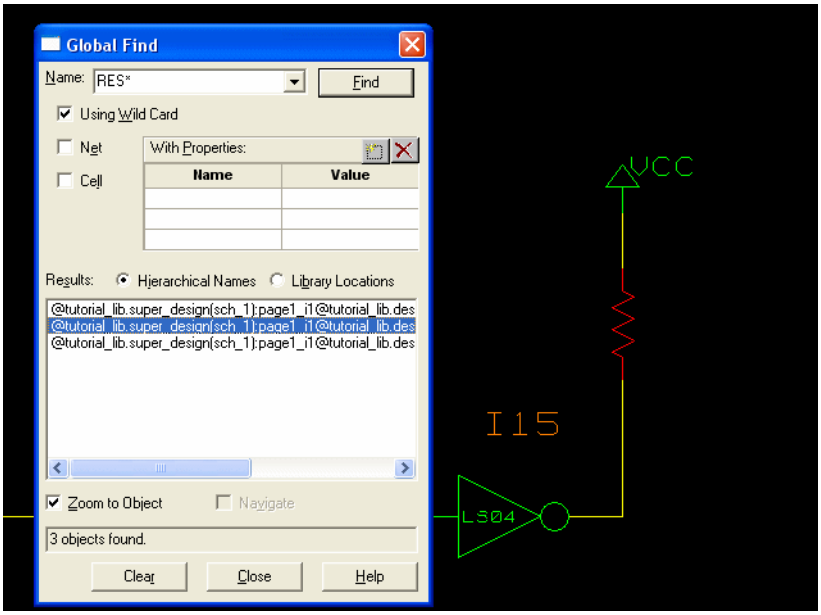
Design Entry HDL highlights the instance in the schematic DESEXAMPLE.SCH.1.2 as shown in the following figure.



Correcting Errors in Assigning Physical Parts

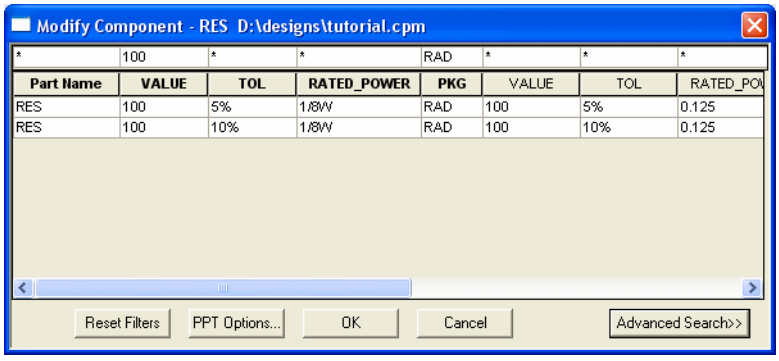
To correct errors in assigning physical parts, follow these steps:

1. Click the second instance of RES in the Global Find dialog box.
2. Design Entry HDL highlights the instance in the schematic DESEXAMPLE.SCH.1.1.



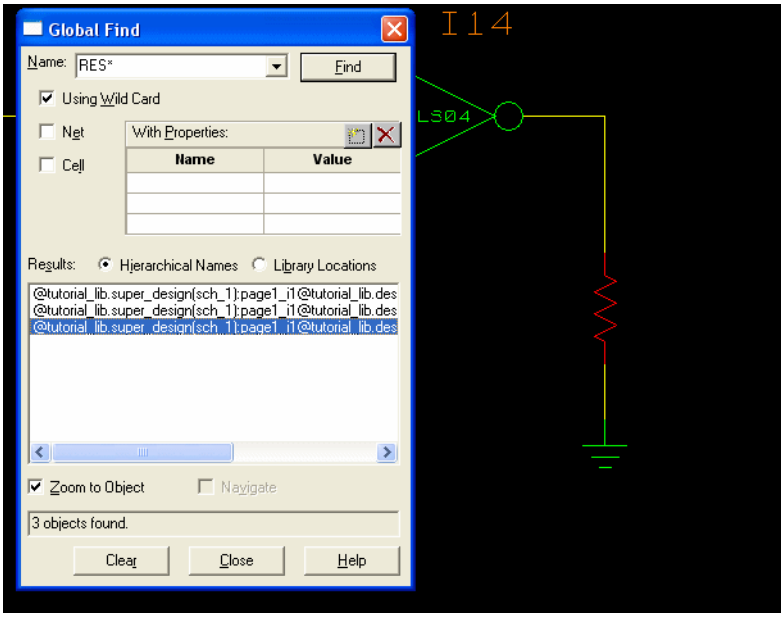
3. Choose *Component – Modify* and click the highlighted instance.

   The *Physical Part Filter* dialog box appears.



4. Click the first row in the Physical Part Filter dialog box.
5. Click *Close* in the Physical Part Filter dialog box.
6. Click the third instance of RES in the Global Find dialog box.

Design Entry HDL highlights the instance in the schematic DESEXAMPLE.SCH.1.1 as shown below.



7. Choose *Component – Modify* and click the highlighted instance.

   The Physical Part Filter dialog box appears.

8. Click the first row in the Physical Part Filter dialog box.
9. Click *Close* in the Physical Part Filter dialog box.
10. Click *Close* in the Global Find dialog box.

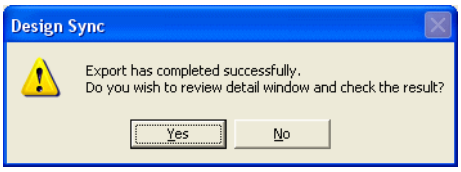
Packaging the Design after Fixing Errors

1. Choose *File – Save*.
2. Choose *File – Export Physical*.

   The *Export Physical* dialog box appears.

3. Select *Repackage*.
4. Deselect the *Update PCB Editor Board (Netrev)* check box.
5. Click *OK*.

Design Entry HDL displays a message window indicating that packaging is complete.



6. Click *No*.

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Multimedia Demonstrations in Design Entry HDL

The following multimedia demonstrations explain important features of Design Entry HDL. Most of the demonstrations listed in the following table that were created or updated before release 16.0 are available on SourceLink. The instructions to access these demonstrations on SourceLink are available on the *Legacy Demos* page of the Allegro Design Entry HDL Help System page. To launch the Help System page, choose *Help – Documentation* in Design Entry HDL, and click the *Demos* tab.

Demo	Objective	Available from...
Displaying Page Names in Hierarchy	Displaying Page Names in Hierarchy Viewer Illustrates how the Design Navigation feature of Design Entry HDL facilitates display of page names in Hierarchy Viewer	CD
Implementing RF-PCB IFF Import	This demonstration shows how to use RF-PCB IFF Import to import a radio-frequency (RF) design into a Design Entry HDL schematic.	CD
Publishing a Design as a PDF Document	To publish a design as a PDF document using the Allegro Design Publisher solution (Publish PDF utility).	CD
Copying a Project using the Copy Project Functionality	To copy a project from one location to another using the *Copy Project* functionality introduced in 15.7.	SourceLink

Copy a Component	To copy a component from one design to another by using Design Entry HDL.	SourceLink
Copy Design to an External Editor	To copy a design to an external editor. The demo also shows how to change capture settings, such as background color.	SourceLink
Copy Image from External Editors	To copy an image created in an external graphics editor to a schematic.	SourceLink
Copy Schematic Objects	To copy schematic objects, such as components, wires, and nets, from one design to another. The demo also shows how to change signal names while pasting a net.	SourceLink
Copy Text	To copy text from an external text editor to schematic. The demo also shows how to retain casing while pasting text.	SourceLink
Getting Started with Component Browser	Provides an overview of Component Browser.	SourceLink
Browsing and Searching for Parts using Component Browser	To search and browse for parts by using Component Browser.	SourceLink
Setting Up QuickPick Browser	To set up the QuickPick browser.	SourceLink
Working with Component Revision Manager	Provides an overview of the interface elements of the Component Revision Manager tool. Also shows how to update schematic instances from your reference libraries	SourceLink
Creating a Project	To create a new project file using Project Manager.	SourceLink
Creating a Schematic	To create a logical schematic by using Design Entry HDL.	SourceLink
Hierarchy Viewer	To highlight the features of the Hierarchy Viewer window. The demo includes procedures for viewing the complete hierarchy of a design, navigating through a design, and reordering modules in the hierarchy.	SourceLink

Import Design	To import sheets across projects. This demo shows how to import designs across projects and change signal names of imported design using the Paste Special dialog box.	SourceLink
Part Manager	To highlight the features of the Part Manager utility. The demo includes procedure for updating part instances on a schematic with appropriate ptf (part table file) rows.	SourceLink
Global Update	To explain how to delete or modify a net, pin, or component property and replace a component in a design.	SourceLink
Cross-referencing a design	To explain how to cross reference a design and read different cross references. The demo includes description of different CRefer reports.	SourceLink
Power Group UI	To highlight the features of the Assign Power Pins dialog box. The demo includes procedures for creating new properties for a component, creating new properties for a group of components, and for passing properties across components.	SourceLink
Design Navigation	Introduces the changes made in Design Entry HDL to display the sheet names along with the block names and page numbers under each block in the design.	SourceLink

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