Allegro®
Design Entry HDL Tutorials and Flows

Product Version 16.0
June 2007

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Contents

Tutorials

The Design Entry HDL documentation consists of the book titles listed below, each of which link to the named online book. The documentation for related tools and methodologies are also listed. Click on a document title to view the document.

Note: If an error occurs and you cannot view the document, you may not have installed the related tool.

Design Entry HDL

Allegro Design Entry HDL Tutorial

Allegro Constraint Manager with Design Entry HDL Tutorial Entry

Front-to-Back Flow

Design Synchronization Tutorial

Allegro Design Entry HDL Reuse Tutorial

Design Variance Tutorial (Available with the Variant Editor tool only)

Related Tools and Flows

Library Explorer and Part Developer Tutorial

Allegro Design Entry HDL Digital Simulation Tutorial

Programmable IC Tutorial

Common PCB Tools and Flows

Common PCB Tools

You can use PCB tools to create quality printed circuit boards for some of the most complex electronic gadgets including motherboards of computers. Based upon your design need, you can select a different tool, or combinations of tools. For example, use Design Entry HDL, a logical design entry tool, to create schematics (logical views). You can use PCB Editor, a physical design tool, to layout and route the physical design. Packager-XL, packages the logical design and generates package files that are used by PCB Editor to generate physical designs.

The more frequently used tools in the PCB toolset are listed below.

Tool	Function
Allegro Design Publisher	Facilitates viewing complex designs made in the Design Entry HDL chematic editor in a Portable Document Format (PDF) file. The design is made viewable independent of the Design Entry HDL application. For more information, see the Allegro Design Publisher User Guide.
Allegro PCB Librarian XL	An advanced library development tool that enables library creation and management by utilizing source-level data standards based on XML. It allows librarians to create, validate, manage, and disperse library part data for use by those using the latest versions of Design Entry HDL schematic in the design entry phase and PCB Editor during the physical layout phase. For more information, see Part Developer User Guide.
Allegro PCB Router	A tool that automatically routes and places the physical design.

Tool	Function
Archiver	A tool that helps create archives of designs and extract a design from a previously created archive. For more information, see Allegro Design Entry HDL Utilities User Guide.
CheckPlus	An electrical design rule checker that automatically detects a wide range of common design errors and oversights that often occur in the design entry process. It also lets you create your own rules. For more information, see Allegro Design Entry HDL Rules Checker User Guide.
Constraint Manager	A tool that provides a spread-sheet based user interface that allows you to quickly capture, modify, and delete constraints. It supports constraint inheritance. It lets you generate reports on constraints captured in the schematic and the board. It also lets you create Electrical Constraint Sets (ECSets). For more information, see the following manuals: ■ Allegro Design Entry HDL - Constraint Manager User Guide ■ Allegro Constraint Manager User Guide
CRefer	A tool that traces the signals in a schematic drawing and annotates their locations with cross references. CRefer also creates schematic reports that contain the list of signal and part cross references. For more information, see Allegro Design Entry HDL Utilities User Guide.
Design Differences	A tool that helps you synchronize following differences between the board and the schematic: ❑ the net, instance, instance part (reference designator), and pin connectivity differences ❑ property differences for instances, nets, or pins ❑ functions, pins, or reference designator swapping differences For more information, see Design Synchronization User Guide.

Tool	Function
Design Entry HDL	A powerful design capture system that fuses robust schematic creation facilities with extensive simulation and verification capabilities. Design Entry HDL is integrated with Constraint Manager to help the high-speed design process. For more information, see the following manuals: ■ Allegro Design Entry HDL User Guide ■ Allegro Design Entry HDL Reference Guide
Library Explorer	A tool that lets you create and maintain libraries, manage library build areas, and launch applications to edit parts and views in a library. For more information, see Library Explorer User Guide.
PCB Editor	A tool for the physical layout system for PCB design. With PCB Editor, you can place and route a design, and then generate the output and documentation necessary for the manufacture of that design. For more information, see Allegro PCB and Package User Guide: Getting Started with Physical Design.
Project Manager	A tool that serves as the interface to the Cadence board design solution from which you can create or open designs and launch tools such as Design Entry-HDL, PCB Editor, and Allegro SI. For more information, see Allegro Project Manager User Guide.
SI	A tool that allows users to explore and resolve electrical performance-related issues at all stages of the design cycle. By exploring and making trade-offs between timing, signal integrity (SI), crosstalk, power delivery, and EMI, designers can optimize electrical performance and reliability before committing the design for manufacture.
SigXplorer	An entry-level PCB interconnect analysis tool available as an add-on option to the PCB Design Studio. It is used to create and edit a virtual prototype of a net topology, simulate the circuit topology and examine the simulation results, explore different circuit topologies until you achieve the desired results. For more information, see Allegro SI SigXplorer Command Reference.

Tool	Function
Variant Editor	A tool that lets you create and manage variants of designs. Each variant has a common base design consisting of a set of core elements that are different from each other by small differences. For more information, see Design Variance User Guide.

Common Flows

To complete any design task, you may require use of multiple Cadence tools. For example, if you need to synchronize the schematic and board, you need to use Design Entry HDL, PCB Editor, Packager-XL, Design Differences and Design Association. All these tools are used in a well-defined flow that requires you to perform specific procedures at different times.

While using Design Entry HDL, you will find the 8 flows (described below) particularly useful. This document lists the 8 flows and provides a brief overview of each flow. At the end of each flow overview, you will find a note that details the path to the Cadence document where you can find more information about the selected flow.

List of Flows Relevant to Design Entry HDL

- Front-to-back Flow
- Working with Electrical Constraints in High-Speed Designs
- Design Reuse Flow
- Design Variance Flow
- Programmable IC (PIC) Flow
- Simulation Flow
- RF Flow
- Team Design Flow

Front-to-back Flow

Front-to-back is the main PCB flow. It involves movement and synchronization of data between the logical design (schematic created in Design Entry HDL) and the physical design (board created in PCB Editor). The main flow moves in two directions:

- Forward mode - In this mode, you create schematic, package the design using Export Physical and use Netrev to take the packaged data to the PCB Editor board. In PCB Editor, you can design the layout and routing.
- Feedback mode - In this mode, you run Import Physical to generate feedback files from PCB Editor. Any changes you made in PCB Editor after initial packaging of the design can be backannotated to Design Entry HDL using Import Physical. You can use Design Differences (VDD) to resolve individual property differences between the schematic and the board. You can update the property differences either to the board or to the schematic.

Note: For more information about the tool used, processes followed, and files generated in the front-to-back flow, see the following books in CDSDoc:

- *Design Synchronization and Packaging User Guide* - See *Chapter 1, Introduction to the Design Synchronization Process* for detailed information.
- *Design Synchronization Tutorial* - This tutorial helps you take a property or connectivity change from the schematic to the board, and perform aback trip. You learn to synchronize both the schematic and the board

Working with Electrical Constraints in High-Speed Designs

As system designs operate at high clock speeds, it has become important to be able to explore the design space upfront at the schematic-entry level. You can pro-actively handle timing and signal integrity issues in Design Entry HDL.

You can assign initial timing and signal integrity constraints using Constraint Manager from within Design Entry HDL. You can also perform simulations and analysis in Signal Explorer and refine these constraints in Constraint Manager. With some constraints already set on the design, the board designer has to make fewer number of iterations while placing components on the board.

Note: For more information, see the *Working with Electrical Constraints in High-Speed Designs* chapter.

Design Reuse Flow

Design reuse is the process of reusing standalone designs in larger designs and thereby reducing costs, building a corporate intellectual property, and increasing the time to market. You can use Design Entry HDL, PCB Editor and Packager-XL to synchronize logical and physical design reuse.

The design reuse flow involves the entire front-to-back flow. At a high level, the design reuse flow is based on two sets of broad steps. First, create a module in PCB Editor for a logical design in Design Entry HDL. You start by defining project settings in Project Manager and creating a design in Design Entry HDL. Next, you package the design and use the packaged files to create a layout. You save this layout as a module and build a logical reuse symbol. Next, reuse the logical reuse symbol in another design and create a layout that uses the module you have created.

Note: For more information, see:

- *Allegro Design Entry HDL Reuse Tutorial* - Use this tutorial to create reusable logical and physical blocks and use them in different designs.
- See the *Design Reuse* chapter in the *Allegro PCB Design Flows* manual in CDSDoc.

Design Variance Flow

You may often require to create designs that have minor variations to existing designs. For example, consider a design AB that has18 resistors, four capacitors, and two shunt terminators, and a design BC that has the same configuration as the design USA with only a small difference in the resistance value of one resistor. In a normal design cycle, you will end redoing the whole design process (from defining part list, creating schematic, packaging design, creating board, and generating manufacturing data) for each variation. Using the Design Variance flow, which involves the use of a tool named Variant Editor, you can create variants of a design from the same base design. You can create assembly drawings and BOM reports for these variants in PCB Editor.

Note: For more information, see:

- *Design Variance User Guide* - Use this guide to learn the basic features of Variant Editor to create design variants.
- *Design Variance Tutorial* - Use this tutorial to try the major features of the Design Variance solution.

Programmable IC (PIC) Flow

Traditional PIC Flow

If you need to implement FPGAs in your designs, you can follow the Programmable IC (PIC) flow. The PIC flow is an integration of Cadence design tools with various place-and-route tools provided by Xilinx, Altera, and Actel. The PIC flow provides the tools for integrating the

Board Design flow with the PIC flow, apart from providing the capability to verify the design at various stages of the design process.

Note: For more information, see the *Programmable IC Tutorial*.

Build Physical Wizard

The Build Physical Wizard allows you to create Design Entry HDL parts using the FPGA implementation files (place and route data (P&R)) data generated by XIlinx, Actel, and Altera, and import these parts into an existing Design Entry HDL board design. The wizard creates a schematic symbol for an FPGA using the place and route data (P&R).

Note: For more information, see

- Select the *Help* button in the Build Physical Wizard.
- See the *Programmable IC Tutorial* in CDSDoc for details on how to use the Build Physical Wizard as part of the overall PIC flow.

RF Flow

You can create a radio-frequency (RF) design using tools such as ADS or MDS by Agilent Technologies, Inc. The ADS tool supports the creation of Intermediate File Format (IFF) files. Once the RF design is ready, you can create IFF files. Both Design Entry HDL and PCB Editor support importing Intermediate File Format (IFF) files. Design Entry HDL supports an IFF interface for importing a schematic IFF file that you can create for your RF schematic, and PCB Editor supports an IFF interface for importing a layout IFF file that you can create for the layout of your RF design.

Once the RF design is ready, you can create IFF files for the schematic and layout of the design. These files can then be used to transfer your design information into Design Entry HDL and PCB Editor.

You can get both graphics and connectivity data of the RF design into Design Entry HDL and then use the RF design as a block in a larger Design Entry HDL design. The interface also gives you the advantage of making concurrent changes in an RF design and then re-importing it into a larger design in Design Entry HDL and PCB Editor.

Important

To run tools, such as hfsymmap.exe, hpfhdl, and updateloc.exe from the command line, you need to do add the following to the variable LD_LIBRARY_PATH:

```
<install_dir>/tools/mainwin501/misc/linux/gcc/fixed3/lib
```

```
<install_dir>/tools/lib
```

The order of the two directories is crucial and should be maintained as such.

Note: For more information, see the *Importing Radio-Frequency Designs* chapter.

Simulation Flow

Design Entry HDL provides a top-down digital design and simulation environment that lets you use multiple simulation engines on the same design. Design Entry HDL supports the digital simulation of designs using:

- Verilog-XL simulator
- Affirma NC Verilog simulator
- Leapfrog VHDL simulator
- Affirma NC VHDL simulator

Note: For more information, see the *Allegro Design Entry HDL Digital Simulation User Guide*.

Team Design Flow

If you need to create a common hierarchical-based design within a large team where each designer owns a block or multiple blocks of the design, then you can use the team design flow to define a common methodology for developing the design.

The team-based design can be completed following an integration area design methodology or using dynamic update. In integration area design methodology, a block is promoted to the integration area after it is ready to be used by other designers. The owner of the block updates the integration area if any changes are made to the block at a later point in time. In dynamic update, multiple team members work on a single project and each team member owns a module of the design. A team member in this approach references design blocks owned by other members as read-only blocks. Any changes made to a reference block by its owner becomes visible dynamically to other members.

Note: For more information, see the *Team Design* chapter.